D3.3

Report on Overall MMIC Concept and Intra-Platform Interfaces

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Abstract:	This deliverable defines the Receive/Transmit architecture for the telecom MMIC-demonstrator and propose the realization of sub-circuits and Intra-platform interfaces
Keywords:	TX/RX, LNA, PA, Mixer, modulator, transition, D-band

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Executive Summary

This deliverable defines the module architecture of the wireless millimeterwave communication demonstrator as well as a steerable antenna based on MEMS-phase shifter, for the M3TERA project. Architecture for the transmitter and receiver (TX/RX) MMIC chipset, based on specifications from telecom industry is defined and concepts/solutions for the realization of the sub-circuits are proposed in detail, including simulations and layout for some circuits (LNA and frequency multiplier). References to published results and a review to the state-of-the-art are given for the sub-circuits of the TX/RX chipset, namely low noise amplifiers, power amplifiers, mixers/modulators, and LO-frequency multipliers. A solution for the non-galvanic transition between the SiGe MMIC-technology and the Si-platform is proposed and analysed by electromagnetic simulation.

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Chapter 1 Introduction

The aim of this report is to give an overview of the general MMIC-concepts for the point-to-point wireless communication demonstrator, to be integrated with the silicon MEMS platform. The report cover design concepts for low-noise amplifiers, power amplifiers, mixers/modulators, frequency multipliers, and intra-platform interfaces, based on the system specifications for the primary application, as given in D1.1. These circuits are the foundation for the MMIC-based receiver and transmitter chipset and all sub-circuits should be proven to work properly before the co-design of full receiver and transmitter MMICs. Our proposed sub circuits, as well the front-end integration, have been successfully verified previously by Chalmers University/Ericsson in a 250 nm InP DHBT-technology, verifying a record high data rate of >50 Gbps by utilizing QPSK modulation. The design strategy in this case was to design for maximum RF-bandwidth and maximum IF-bandwidth, with a minimum of gain variation, and good input/output matching. For the SiGe based designs in the M3TERA-project, the same concept will be followed, thereby minimizing the risk of failure due to frequency shifts, etc. The frequency range of interest is 140-150 GHz as first priority, and as a second priority 220 GHz center frequency. To minimize the risk, integration of oscillators (for the LO), IF-amplifier, and PLL-circuits will not be done in this project. The RX/TX chipset is also proposed to be designed for maximum flexibility to allow for direct modulation, SSB receive/transmit, dual conversion etc. Some circuits were submitted for fabrication already in April 2015, simulation results from this design round are reported here as well.

Chapter 2 Block diagram for D-band RX/TX chip-set

Based on the system specification of the primary application, a P-t-P link for wireless backhaul, as described in D1.1 of the MTERA-project, a block diagram for the Receiver (RX) and Transmitter (TX) is proposed (Figure 7 in D1.1). The target RF-frequency is between 140-150 GHz. This coincide with US FCC allocation plan for 'fixed and mobile communication', in the frequency band 141-148.5 GHz (this is a part of the D-band 110-170 GHz).

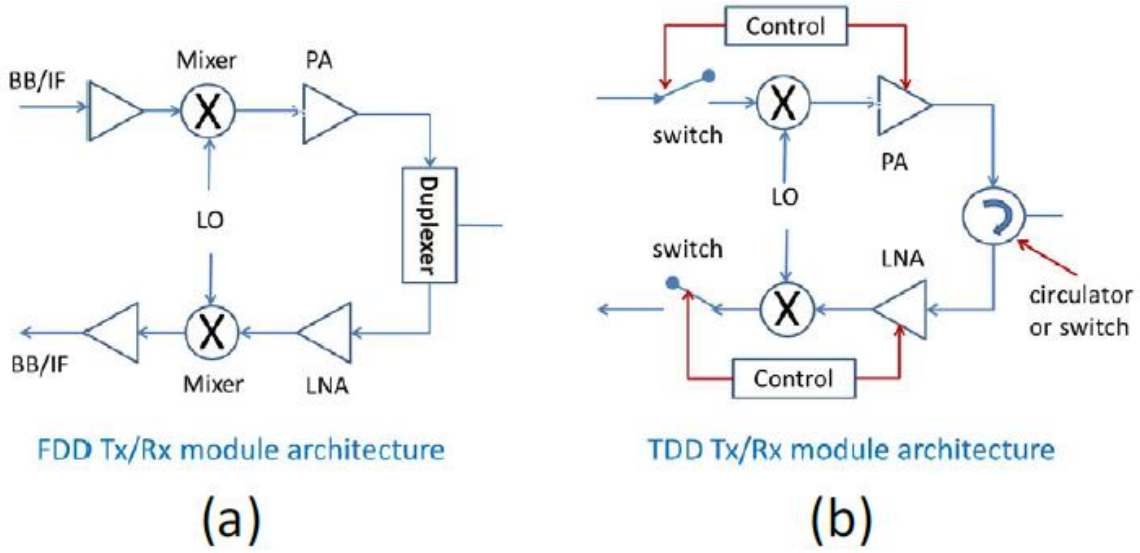

Figure 1: Block diagram for FDD and TDD RX/TX architectures as given in D1.1

Circuits to be implemented in the M3TERA for the D-band RX/TX chipset are as follows

- Low noise amplifier for the receiver, LNA
- Power amplifier for the transmitter, PA
- Mixer/modulator for the receiver and transmitter, RXMXR, TXMXR
- Local oscillator chain for the receiver and transmitter, LO-X6 frequency multiplier

Assuming FDD architecture, as was proposed in D1.1, specs according to Table 1 are proposed.

Table 1: Specifications for primary sub-circuits

circuit	NF (dB)	P_{sat} (dBm)	Gain (dB)	LO-RF Isolation	I-Q imbalance
LNA	10	>0 dBm	20		
PA	<20	10 dBm	20		
RXMXR	15	TBD	0		TBD
TXMXR	15	-5 dBm	0	>25	TBD
LO-X3(X6)	-	2-5 dBm	2-5 dBm		

The RX/TX chipset is proposed to consist of a combination of the above listed circuits, according to Figure 2 and Figure 3.

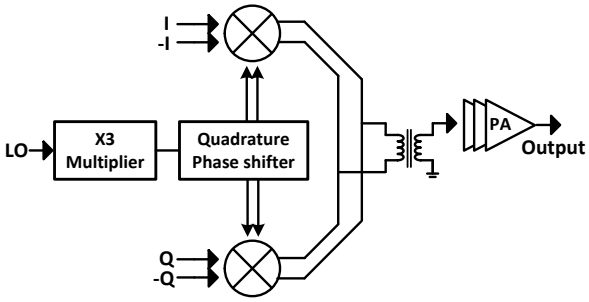

Figure 2: TX Block diagram

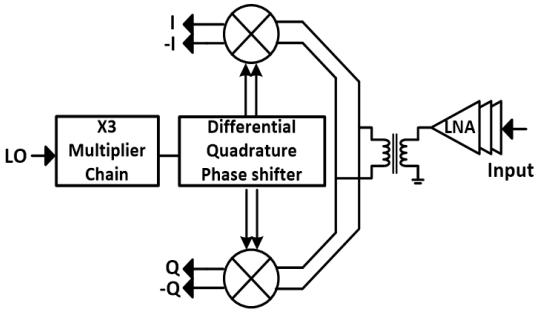

Figure 3: RX Block diagram

As first priority circuits we propose to implement the mixers as I-Q mixers, utilizing a double balanced Gilbert-mixer topology [2.2], and using frequency multipliers for the LO-chain, either x3 or x6 frequency multipliers [2.3]. This concept allows us to use an external oscillator, herewith we reduce the risk of frequency shifts, and possible excessive phase-noise of the oscillator. This concept was previously used for a D-band RX/TX chipset which achieved record-high data rate [2.1]. The target baseband bandwidth of the mixers should be more than 5 GHz in order to cover the 140-150 GHz frequency band, assuming direct modulation with 4 GBaud symbol frequency, see Figure 4. By using existing modems from Ericsson, a full duplex link could be demonstrated as an alternative to direct modulation and TDD. The frequency allocation would then as an example look like Figure 5. In this case the bandwidth is 250 MHz, but depending on the continuous development of new modems this bandwidth will most likely increase to 500 or even 1000MHz in the near future. Duplex filters are needed to separate the RX and TX-bands. In this particular case, receive and transmit frequencies are separated as much as possible. For the purpose of functionality test, however, we propose to demonstrate a one-directional hop utilizing one transmitter and one receiver, without the duplex filter.

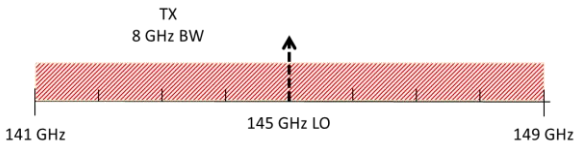

Figure 4: Typical RF-spectrum assuming direct modulation

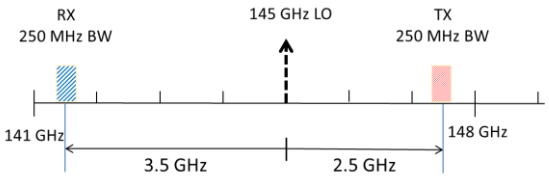

Figure 5: Typical RF-spectrum assuming sub-carrier modulation

With a x6 frequency multiplier on the LO-chain, the external oscillator frequency should be 24,17 GHz for a mixer LO-frequency of 145 GHz. Such external oscillators can be considered to be COTS. This also applies to the IF-amplifiers. Therefore these circuits have secondary priority. Alternatively, an x4 frequency multiplier could be added (giving a total LO-multiplication factor of 24) with the VCO at 6 GHz. There is however a risk that spurious frequencies might deteriorate the performance with such a low input frequency. Secondary priority MMICs are listed according to Table 2 with key specs.

Table 2: Specifications for secondary sub-circuits

circuit	Freq GHz	BW GHz	NF	Gain	PN @100kHz	Unwanted harmonics	Pout dBm
X4	6 to 24	1		0dB		-30 dBc	0
VCO	5.8-6.3	0.5			-110 dBc		0
IF-ampl	0,1-5	>5	<2 dB	>20 dB			0

References:

2.1 S. Carpenter, Zhongxia He, Mingquan Bao, H. Zirath, ' A Highly Integrated Chipset for 40 Gbps Wireless D-Band Communication Based on a 250 nm InP DHBT Technology', 2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICs)

2.2 S. Carpenter, M . Abbasi, and H. Zirath, "Fully Integrated D-Band Direct Carrier Quadrature (I/Q) Modulator and Demodulator Circuits in InP DHBT Technology," IEEE Transaction on Microwave Theory and Technique, May 2015.

2.3 M. Bao, R. Kozhuharov, H. Zirath,'A High power-efficiency D-band frequency tripler MMIC with gain up to 7 dB', IEEE Microwave and Wireless Components Letters, Vol. 24, no 2, pp 123-125, 2014.

Chapter 3 Block diagram for steerable antenna design

Antenna array is an overwhelming hot topic today in context with the development of fifth generation (5G) wireless technologies where arrays with 100+ antenna elements are considered for multiple UE beamforming. In this project, however, we consider only applications where simple beam steering is required, because the response time[1] of any tuning devices based on micromachined mechanical structures is too large for wireless access use scenarios.

One use case is antenna alignment in millimeter-wave (mmW) point-to-point (PtP) links. At high frequencies, high gain antennas are used to compensate large path loss and rain attenuation, resulting in extremely narrow antenna beams which makes the antenna alignment difficult during installation. Another use case may be the PtP links for small cell backhaul and front-haul. Unlike macro-sites, small cells can be expectedly installed on less-stable structures a few meters above street level, e.g., on lampposts. Beam steerable antennas may be used to dynamically compensate the post sway caused by wind. A concern with this second use case is the reliability and lifetime of the micro machined structures which has to be constantly activated/de-activated during the lifetime course of the radios. This issue will be investigated while the project proceeds. So, automatic alignment of mmW PtP links is chosen as the basic application of the steerable antenna for the moment.

There ways exist to implement a steerable antenna system: analog phased array, digitally tuned (phase or time) array, and hybrid of the analog and digital implementation. We are limited to the analog implementation, since micro machined D-band (150 GHz) phase shifters will be used as the tuning elements. Figure 6 shows the conceptual block diagram of a beam steerable antenna system to be developed in this project. It also indicates the deliverable where the corresponding blocks will be defined or developed.

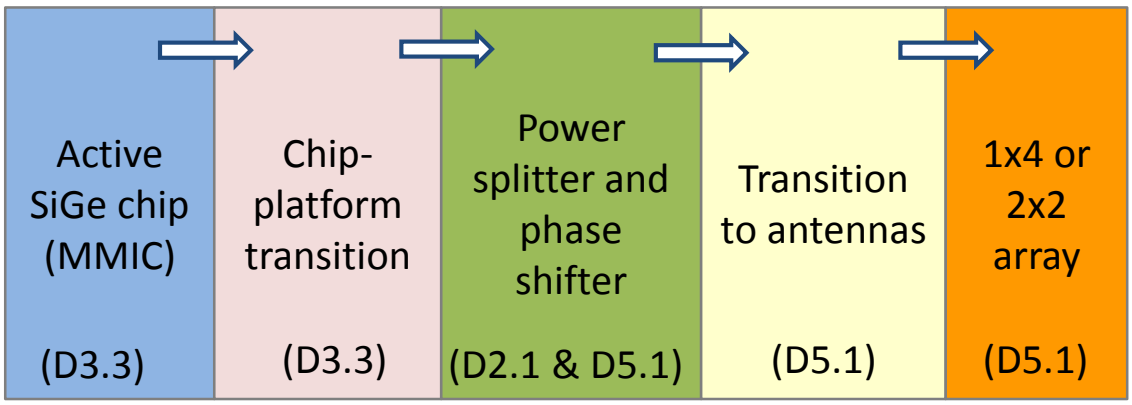

Figure 6: Conceptual block diagram of a beam steerable antenna system. Also given are the deliverables where the corresponding blocks will be defined or developed

[1] Normally on the order of 10 ms

The active chip (MMIC) is defined in this chapter and will be designed in WP3. The chip-to-platform transition is defined in this report (see Chapter 3). The micro machined power splitter and phase shifter will be defined in D2.1 and D5.1. Finally, interface between the platform and the antenna will be defined in D5.1 by KTH and Ericsson.

For current deliverable, we focus on definition of the SiGe chip to be used in the beam steerable antenna sub-system. Our goal is to design a multiple function MMIC which contains a frequency multiplier, a D-band on-chip band pass filter, and an amplifier, as depicted in Figure 7.

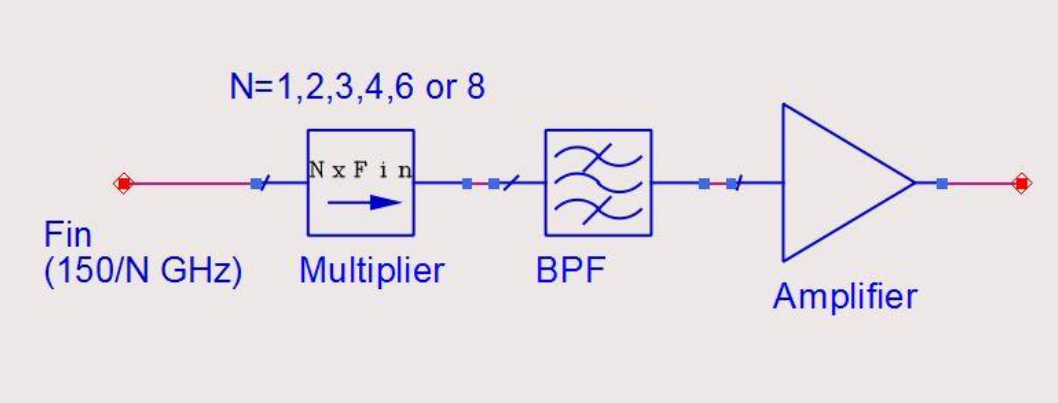

Figure 7: Block diagram of the active chip to be used in the beam steerable antenna sub-system

The input frequency, Fin, is 150/N GHz, where N=1, 2, 3, 4, 6 or even 8, depending on which multiplier factor will be chosen. The final N will be decided later when further simulation work is done. When N=1, it means that a 150 GHz signal will be applied at the input directly, so the multiplier and filter may be excluded.

Since this demo is to mainly test the power splitter and the phase shifter as well as the transition to the antennas, the absolutely power level from the amplifier is not critical. Output power from 0 to +5 dBm should be fine.

As a backup solution and a measure to risk management in case the SiGe chip should fail in some way, a chip that consists of a passive transmission line will be included in the first design tape-out, as sketched by Figure 8. Whether it will be a micro-strip or coplanar waveguide will be determined later when we know better which one facilitates the chip-to-platform transition design better.

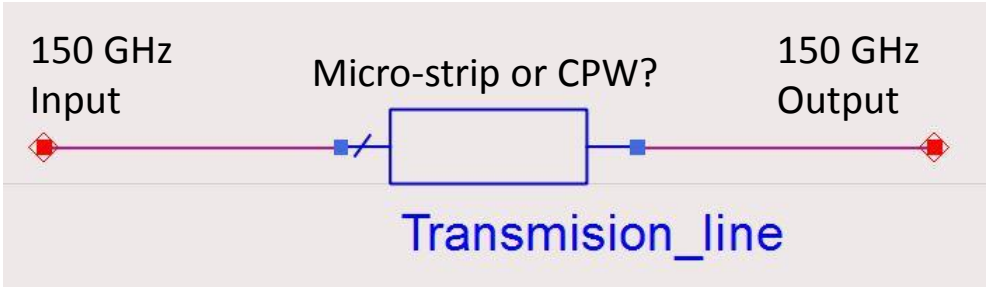

Figure 8: A chip containing only a passive transmission line will be included in the design as a backup solution

Chapter 4 Conceptual circuit designs

This chapter review the state-of-the-art for SiGe HBT-based active circuits, needed for the M3TERA-project, such as low-noise amplifiers (LNA), power amplifiers (PA), mixers, and frequency multipliers for the LO-chain. These circuits will be designed and manufactured in the B11HFC-process by Infineon in a first phase. In the second phase, a receiver and transmitter will be co-designed using the knowledge gained from phase 1.

4.1 Amplifiers

4.1.1 Review of state-of-the-art D-band LNA and PA's from the research literature

Various amplifiers will be needed for the receiver chip (LNA) and the transmitter chip (PA) with specifications according to Table 1 and Table 2. Early work [4.1.1-4.1.2] show promising performance in D-band utilizing a SiGe technology having f_T/f_{MAX} of 230/300 GHz. A five stage 140 GHz amplifier was demonstrated, see Figure 9.

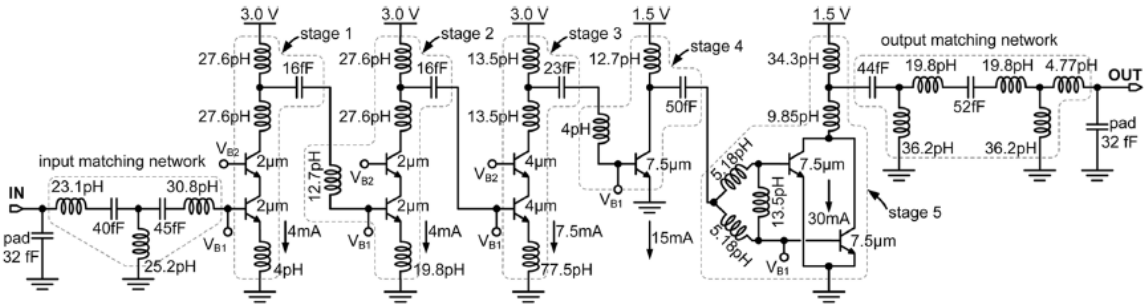

Figure 9: Circuit topology of five stage amplifier from ref [4.1.1]

The amplifier consists of three cascaded cascodes followed by two CE-stages. Emitter inductive degeneration is used on the cascade stages, thereby increasing the real part of the input impedance for that stage. The final stage consist of two paralleled stages, each having an emitter length of 7.5 µm. Measurements, see Figure 10, shows a gain of more than 10 dB from 125 to 145 GHz with average at 18 dB at 25 C. Output power is -3 dBm at 1 dB compression, measured at 130 GHz. P_{sat} is $1dB_m$. All transistors are biased at a current density of 14 mA/µm^2 at peak f_T. Devices have 130nm emitter width. A noise figure of 12.3 dB was demonstrated for a receiver based on this LNA.

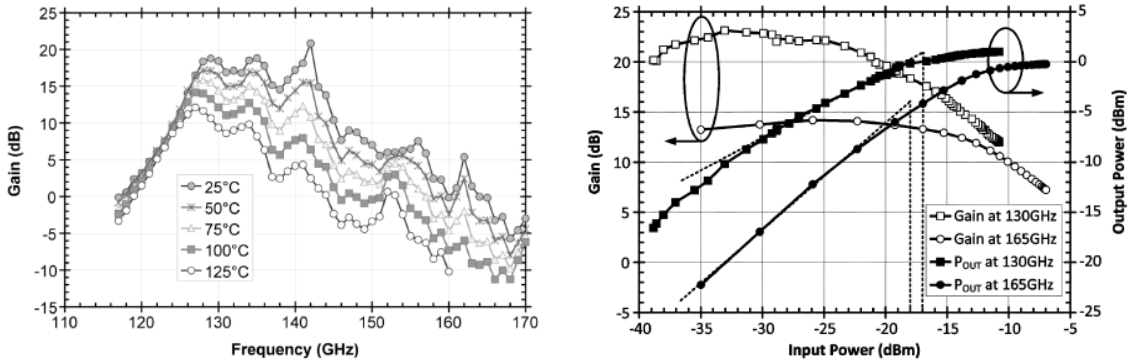

Figure 10: Measured gain variation over frequency and temperature, and measured output power at 130 GHz. From ref [4.1.1].

Recently a D-band LNA was demonstrated utilizing a 90 nm BiCMOS process (IBM9HP) having f_{MAX} and f_T of 350/300 GHz [4.1.3]. The LNA consist of three cascade stages and a final CE-stage. This LNA shows excellent performance with 30 dB gain, a 3dB bandwidth of 30 GHz and a noise figure of 7.5 dB from 120 to 150 GHz.

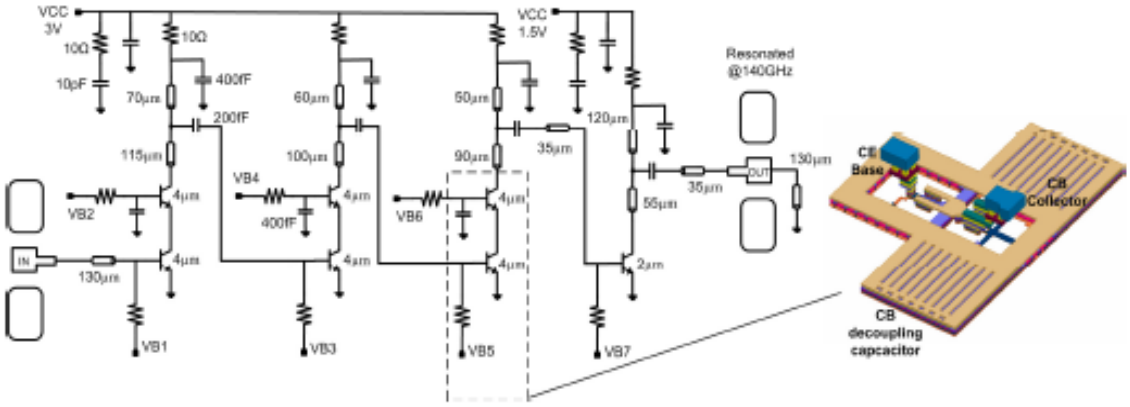

Figure 11: LNA schematic from [4.1.3].

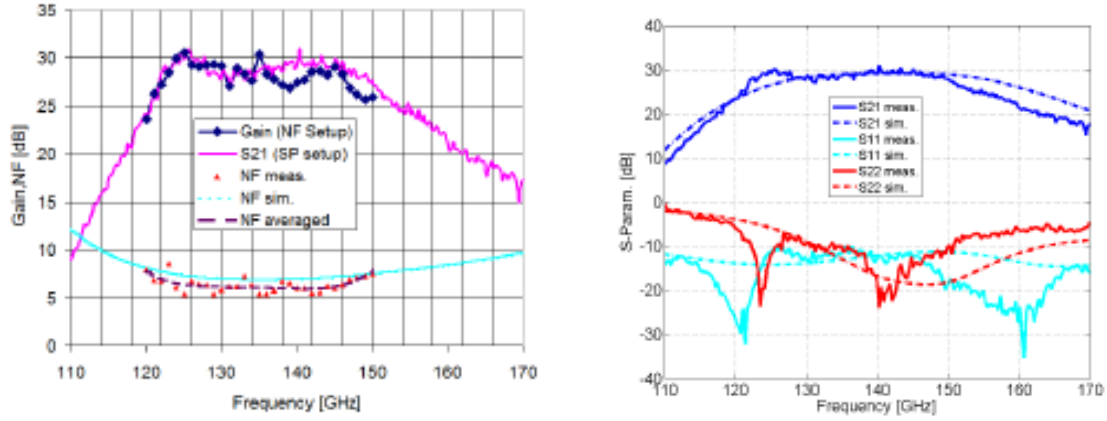

Figure 12: Measured and simulated gain, noise figure and S-parameters, from [4.1.3].

A similar approach using cascaded cascodes was used in ref [4.1.4]. This circuit use current mirrors for the biasing, see Figure 13. The process is IHP 0.13 μm SiGe.

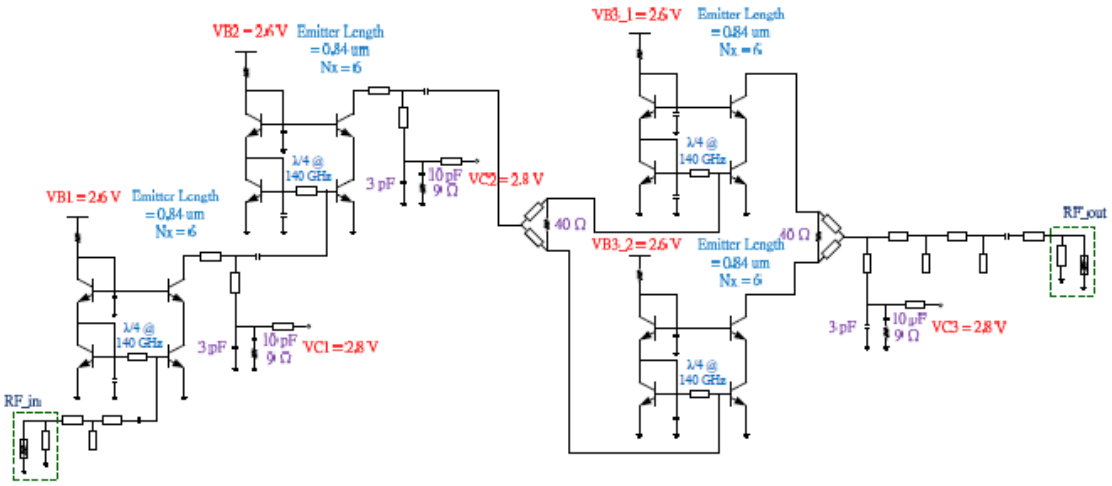

Figure 13: Schematic of broadband amplifier described in [4.1.4] utilizing current mirrors for biasing.

The measured and simulated gain and return loss is shown in Figure 14.

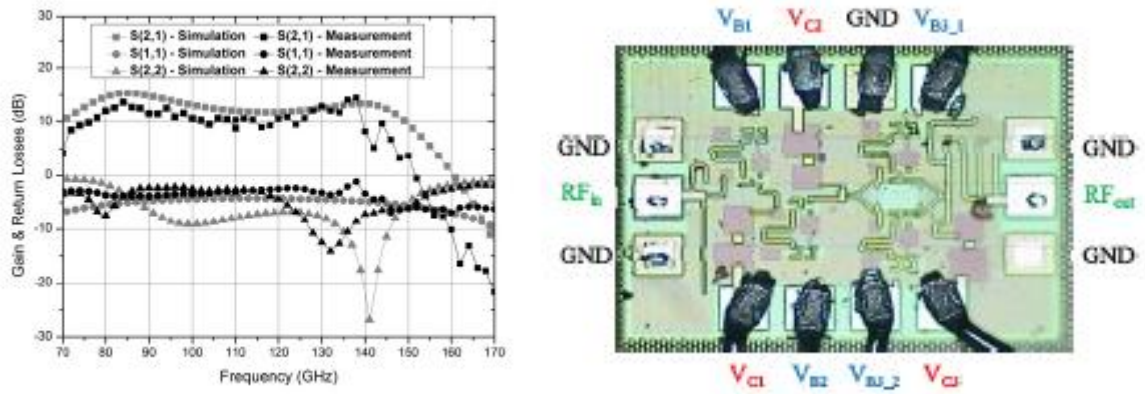

Figure 14: Measured and simulated gain and return loss, and chip photo. From [4.1.4].

This chip has a gain bandwidth product of 231 GHz.

Regarding power amplifiers, most designs are realized as balanced amplifiers with input and output baluns to convert single-ended to balanced. In [4.1.5], a 160 GHz PA is demonstrated, utilizing a 3-stage balanced cascade topology, see Figure 15 and Figure 16 shows the measured S_{21} , P_{1dB} (8.2 dBm) and P_{SAT} ($10dB_m$).

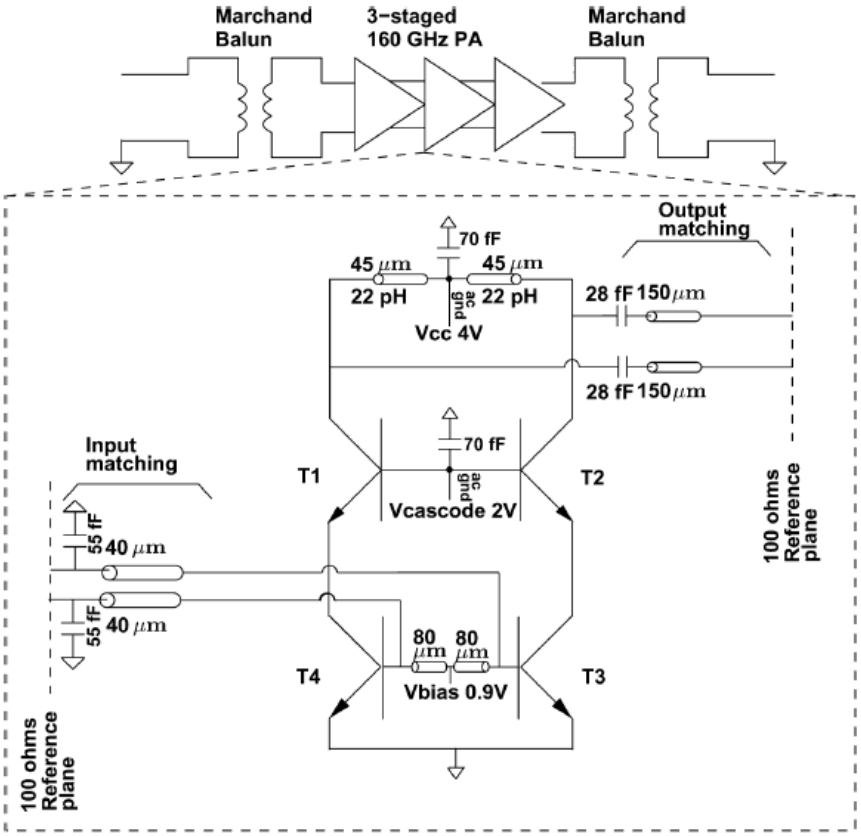

Figure 15: 160 GHz PA described in reference [4.1.5].

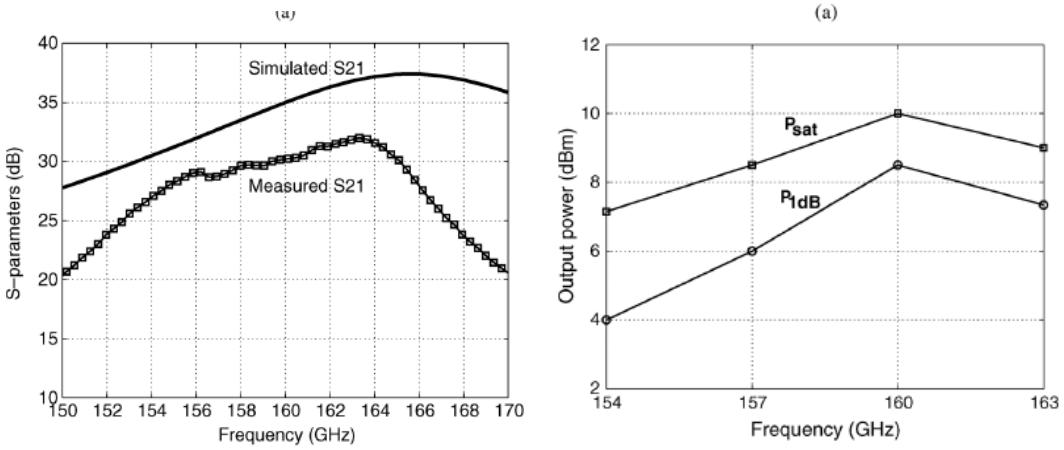

Figure 16: Measured S21 and Psat, P1dB of design in reference [4.1.5].

A similar approach is demonstrated by Yishay and Elad in reference [4.1.6] realized in IBM's 0.12 μm SiGe BiCMOS8XP-process. The D-band PA consist of three balanced, cascaded cascodes, see Figure 17 and Figure 18.

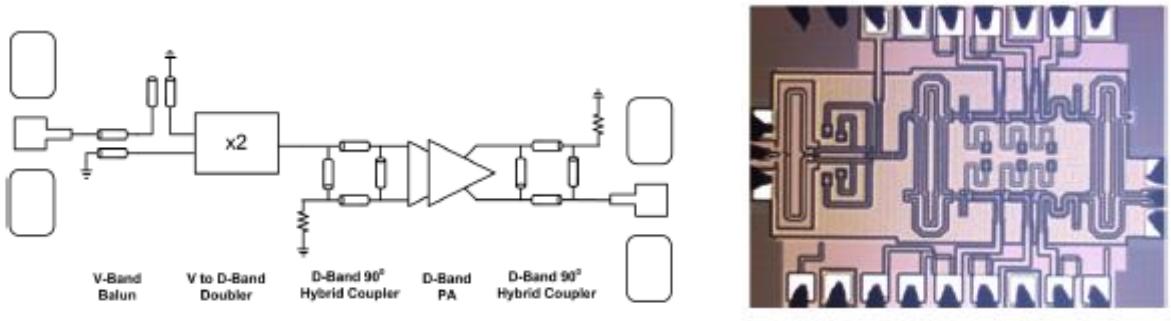

Figure 17: Block diagram and chip photo of frequency doubler + D-band PA from [4.1.6]

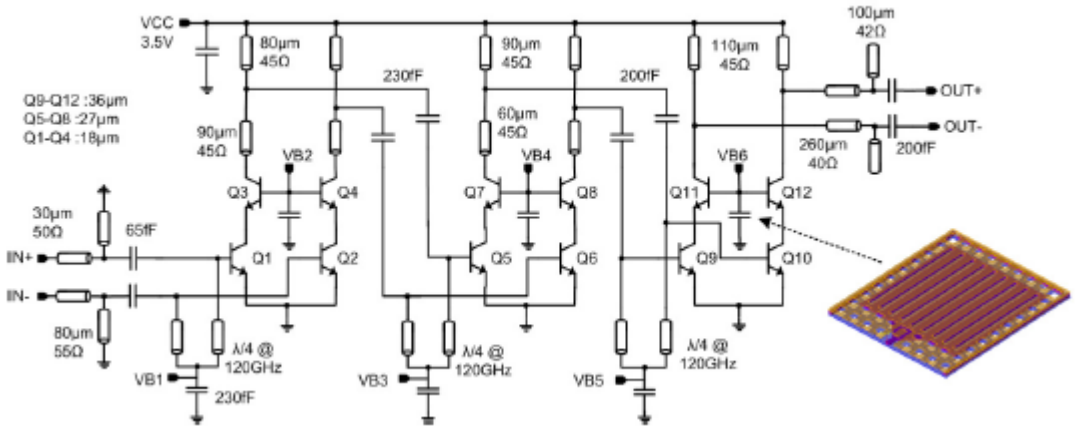

Figure 18: Schematic of D-band PA, from [4.1.6]

The measured PA-breakout shows a gain of approximately 30 dB from 110 to 125 GHz, and a saturated output power of 17.4 dB_m, see Figure 19.

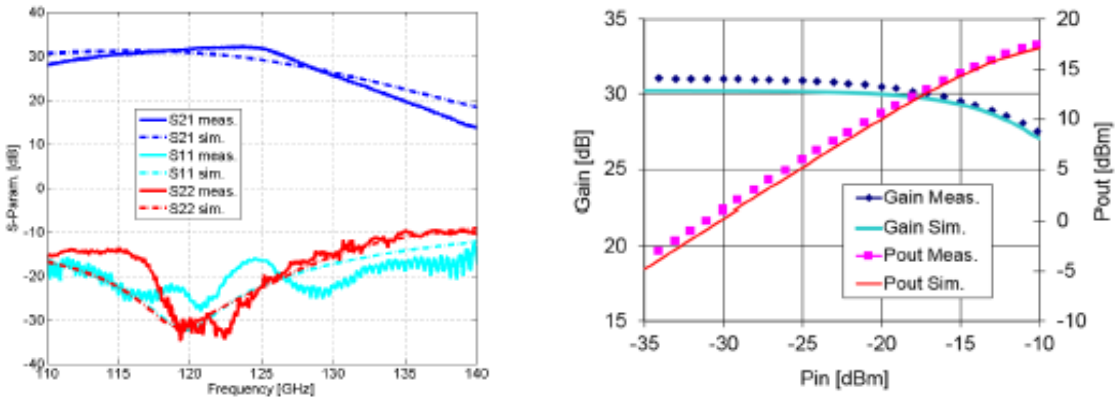

Figure 19: S-parameters, gain and output power at 120 GHz, from [4.1.6]

The so far highest reported output power in D-band is presented in ref. [4.1.7]. The power amplifier combine the power from 8 amplifiers, each capable of delivering >10 dB_m from 114-134 GHz with a peak power of 13.8 dB_m at 126 GHz. The schematic for the single amplifier is shown in Figure 20.

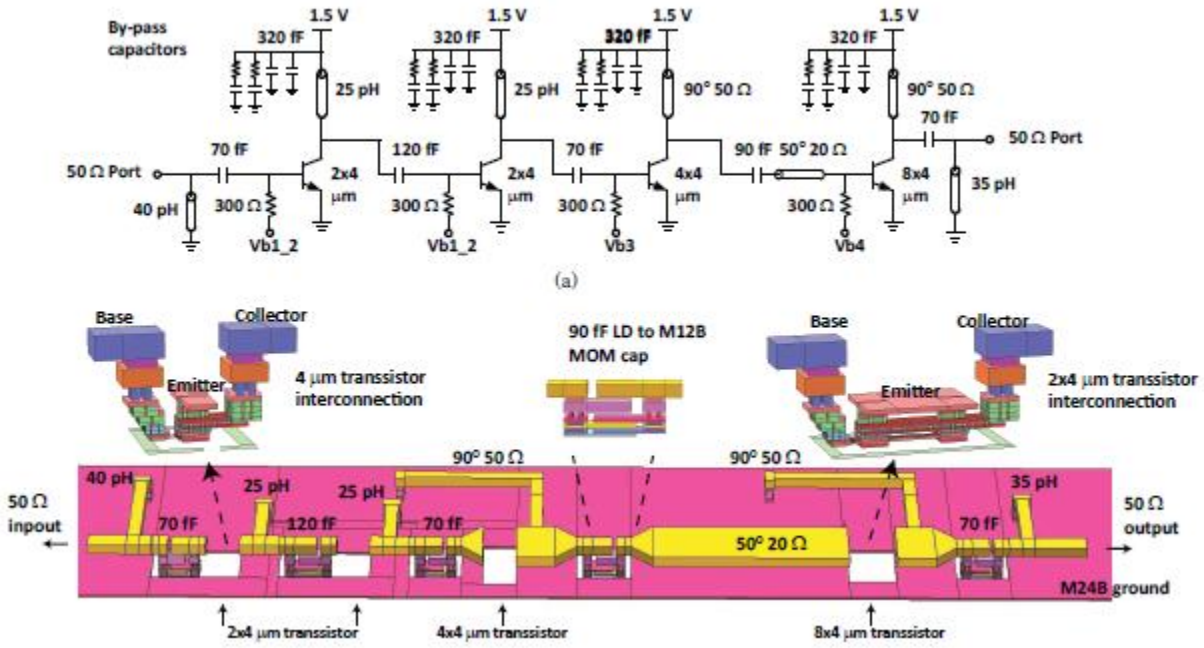

Figure 20: Schematic and layout of single ended PA from ref. [4.1.7].

The power from the 8 amplifiers is combined in an 8-way combiner, as shown in Figure 21 Quarter wave microstrip lines are used for impedance matching to 50 ohm. The PA is realized in the IBM 9HP BiCMOS process with 10 layer copper backend.

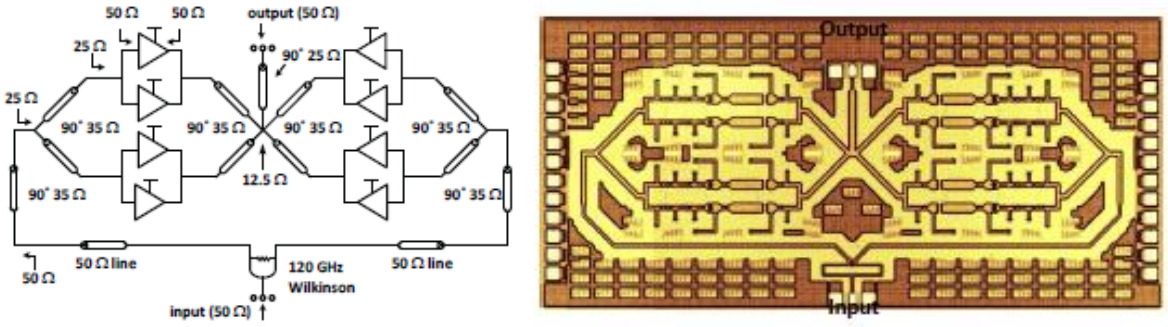

Figure 21: Schematic of the 8-way power combining amplifier and chip photo (ref. [4.1.7].)

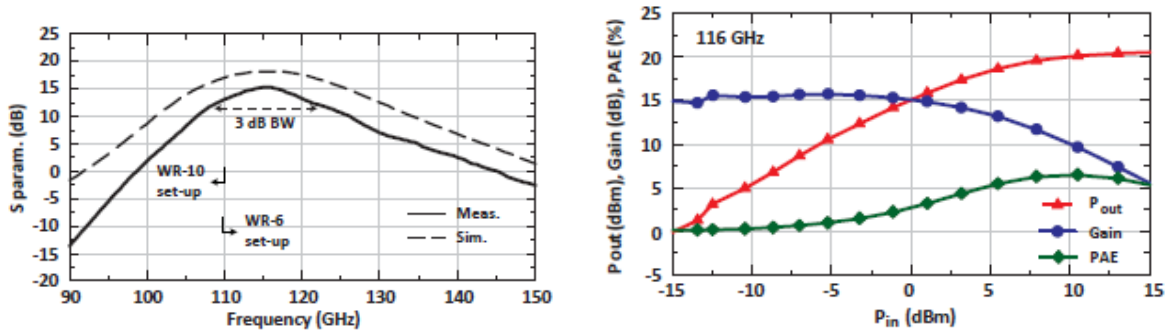

Figure 22: Measured and simulated gain and measured output power at 116 GHz, (ref. [4.1.7].)

For the M3TERA project, the design strategy is to achieve a wide bandwidth and maximum flatness in order to minimize the risk of frequency shift due to process variations and inadequate modeling of devices and their parasitics. One solution to this problem is to use low-Q matching techniques, as described in [4.1.8] and [4.1.9]. The basic principle is to lower the Q-value of the inter stage matching circuit in order to increase the bandwidth, Figure 23.

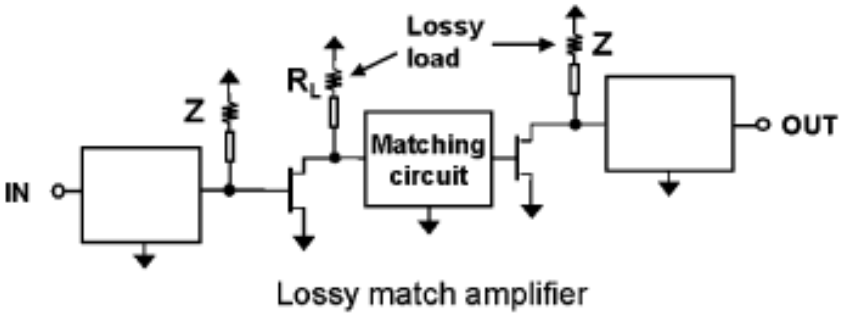

Figure 23: Basic concept of lossy match amplifier (from [4.1.9]). By introducing a lossy load at the output of each transistor, the Q-value is decreased and, consequently, bandwidth can be increased.

This can be applied to the input and output matching circuits as well as the interstage matching shown in Fig. 4.1.16. Multi octave bandwidth, with maximally flatness and constant group delay has been demonstrated by utilizing this concept. Instead of using single transistors in common source or common emitter configuration, cascade cells can be used in order to increase the gain per stage.

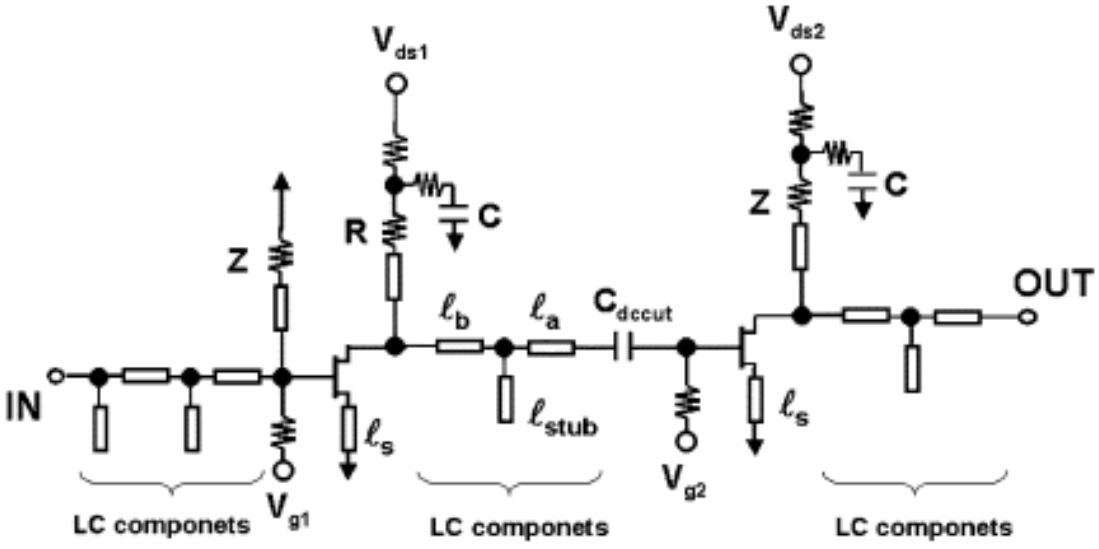

Figure 24: Example of realization of the basic concept described by Figure 23 (from [4.1.9]). A source inductance (l_s) is introduced in order to increase the real part of the input impedance, matching elements are realized as transmission line stubs.

4.1.2 D-band amplifier work done in M3TERA project until Sept 2015.

The lossy-match concept was implemented as a 6-stage lossy match amplifier topology in B11HFC, a layout was also generated, see Figure 25. A very high1dB bandwidth of 117-162 GHz was achieved with a nominal gain of 18.9 dB. The simulated noise figure is 10.2 dB. S-parameters and noise figure is shown in Figure 26in the frequency range 100-200 GHz.

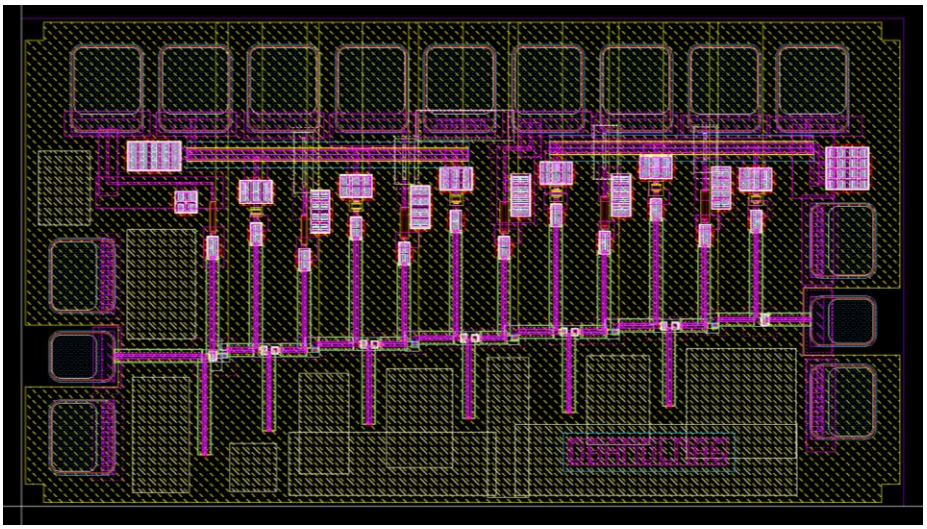

Figure 25: Layout of the lossy match 6-stage D-band amplifier, 945x512 □m2

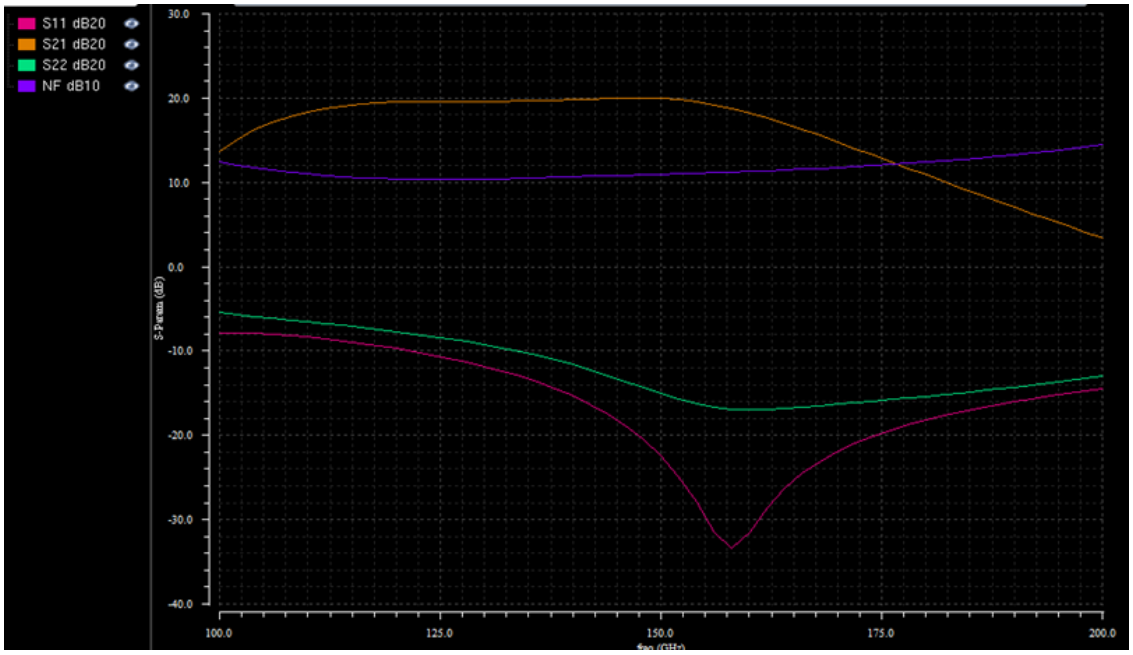

Figure 26: Simulated S-parameters and noise figure for the 6-stage D-band LNA from 100 GHz to 200 GHz.

A Cascode design was also explored, with 3 stages (2 cascode stages followed by a CE-stage), a gain of 18.5 dB was achieved with a noise figure of 9.8 dB, see Fig 4.1.20. The 3dB bandwidth is 126-160 GHz. The layout is shown in Figure 27.

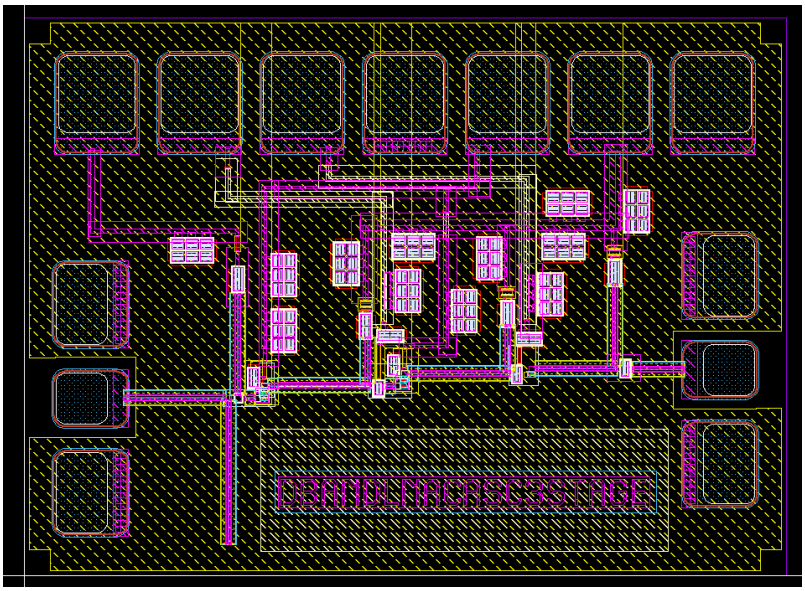

Figure 27: Layout of the lossy match 3-stage D-band amplifier.

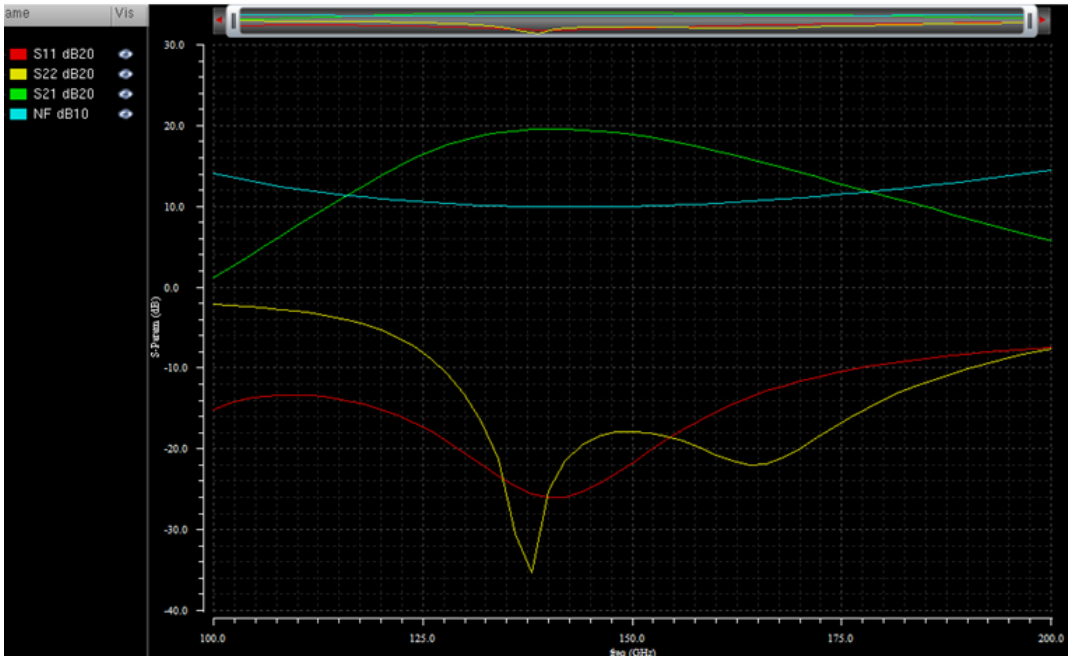

Figure 28: Simulated S-parameters and noise figure for the Cascode D-band LNA from 100 GHz to 200 GHz.

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4.2 Mixers

4.2.1 Direct frequency Conversion design for single chip integration

Direct conversion and super heterodyne are commonly used frequency conversion architectures in wireless systems. The two-step, or super-heterodyne, transceiver can also be described as the linear shift of signal frequency where one or more intermediate frequencies (IFs) are used in order to relax the specifications of individual circuit blocks [4.2.1]. Although a two-step transmitter architecture shows good promise for higher performance, the architecture does have some drawbacks with respect to single-chip integration. Larger number of components and interconnects may lead to unwanted internal coupling of the signal as the frequency increases. Increased power consumption may increases the temperature of the chip and results in unwanted effects. Finally, the larger chip area is not favorable when prices and large scale integration are of concern.

In a direct conversion transmitter, the information is directly placed on a carrier at the signal frequency of transmission. This carrier is generated by the local oscillator. Since the modulating signal is located at zero frequency, no undesired sideband is generated in the process of modulation. This simplifies the architecture since no additional filtering will be needed. The output signal from the direct carrier modulator should normally be amplified before it is transmitted.

4.2.2 Design Challenges and solution for direct frequency conversion Mixers

Direct conversion up converter suffers from an important drawback of carrier leakage through the mixer [4.2.2], [4.2.3], [4.2.4]. This unwanted signal is located within the band of the

transmitted signal and cannot therefore be avoided by means of filtering. The major problem which is caused by leaking LO signal is what is known as LO pulling. The leaked LO signal is usually a large signal and drives the power amplifier into its nonlinear operation region. The biggest concern in direct conversion receiver is the low frequency noise generated by the electronic components, especially the baseband amplifier [4.2.5]. Also, any part of the LO signal which leaks to the input of the receiver, mixes with itself and becomes a dc components. This dc signal is in the same band as the information signal and can effectively reduce the signal to noise ratio.
The above problems in direct frequency conversion mixer can be solved by improving port isolation using double-balanced Gilbert mixer cells and this topology also increases higher conversion efficiency. As shown in the schematic diagram of Figure 29, two of such mixers are fed with orthogonal carriers and the outputs are added in the current domain and passed through a common inductive load. A 150-168 GHz transmitter is designed using I/Q mixers in 0.25μm SiGe HBT technology in [4.2.6] .

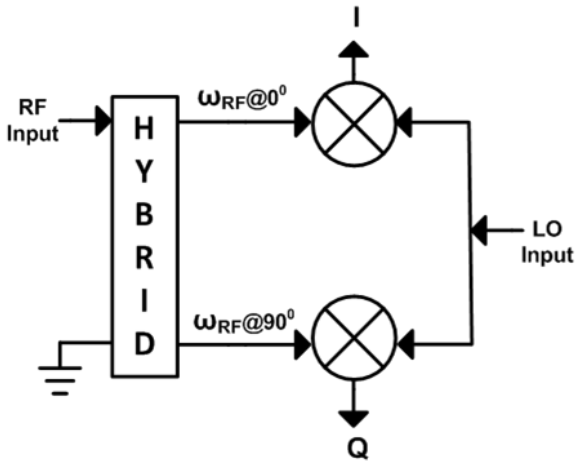

Figure 29: Two variation of demodulator topology depending on 90 degree hybrid location where each mixer is a double balanced Gilbert cell mixer. Modulator topology is reversing the RF and IF ports.

A basic down conversion Gilbert mixer is shown in Figure 30. This cell involves two parts, input stage and switch stage. The input stage is often called transconductance stage which converts the RF voltage signal to a current signal and consists of transistors Q_1 and Q_2. The second part is the switching core driven by the local oscillator and changes the polarity of the RF current at the rate of LO frequency. Millimeter wave receivers are designed in SiGe technology in the D band frequency range in [4.2.7], [4.2.8], [4.2.9].

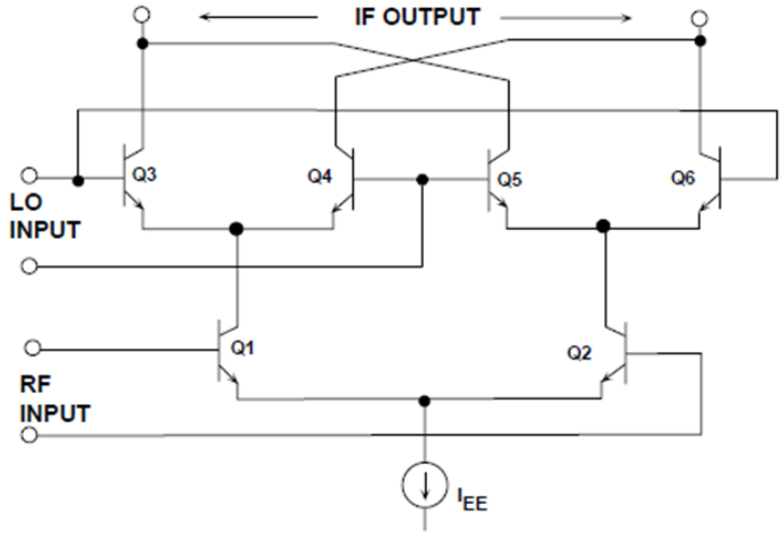

Figure 30: The classic Gilbert cell active mixer

The direct conversion receiver can also be used as an image reject mixing stage. The I and Q signals will contain both the upper and lower sideband signals but with 90 degree phase difference. An additional phase shifter can be used to separate these sidebands. Quality of this separation depends on the phase balance of the two carrier signals.

Similarly direct conversion transmitter can therefore also be used as a single-sideband up-converter where there will be no need for additional filtering as required in two step conversion. The sideband suppression will be used as a measure to amplitude and phase imbalance. Depending on the modulation format and system requirements additional correction may be applied to remove the phase and amplitude errors. Numerous analog and digital methods for I/Q mismatch correction are available [4.2.10], [4.2.11], [4.2.9].

A D-band (110–170 GHz) monolithic microwave integrated quadrature up- and down-converting mixer circuits with on-chip RF and local oscillator (LO) baluns are designed and characterized in [4.2.13] [4.2.14]. The circuits are fabricated in 250-nm indium–phosphide double heterojunction bipolar transistor technology. The mixers require an external LO signal and can be used as direct carrier quadrature modulator and demodulator to implement higher order quadrature amplitude modulation formats. The modulator layout is shown in Figure 31.

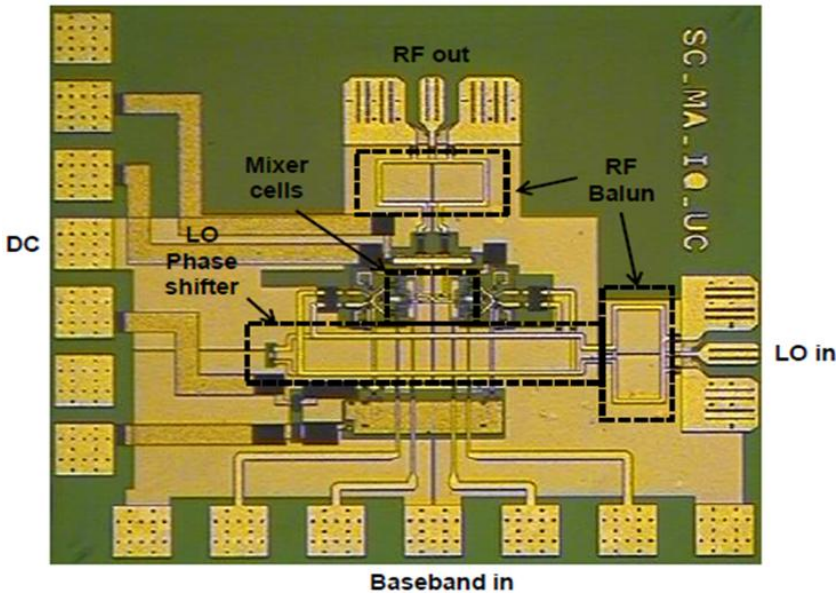

Figure 31: Chip photograph of the IQ mixer. The active chip area including the RF baluns is 560µm× 440µm.

The design is tested with a CW input signal at 1 GHz and 0 dBm LO power and exhibits up to 6 dB conversion gain and more than 22 dB image rejection ratio. The LO signal is suppressed by more than 27 dB. The chip consumes 78 mW DC power and can provide up to 3 dBm RF power in saturation. The active chip area is 560µm× 440µm.
Apart from selecting the size of the transistors and their bias currents, proper implementation of passives structures and their modeling accuracy becomes increasingly important for design success at millimeter waves. Unlike conventional transmission line based matching techniques, custom spiral inductors are implemented and used together with MIM capacitor of the process to perform impedance matching in this design. By taking advantage of the multilayer stackup, this approach significantly reduces the consumed chip area. All other interconnects, even though being very short are modeled as transmission lines and their effects are included in the simulation. These components are EM-simulated in HFSS and imported into the circuit design environment for co-simulation.

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4.3 Frequency multipliers

4.3.1 Technical challenge of frequency multipliers

A LO signal source for a D-band transceiver is not commercial available. A frequency multiplier chain has to be used to convert a low frequency signal into a high frequency one (D-band). For example, a frequency multiplier-by-six (x6) can convert a K-band signal at 24.0 GHz into a D-band signal 144 GHz. Usually, the multiplier chain consists of a frequency tripler, a frequency doubler, as well as a buffer amplifier, as shown in Figure 32 [4.3-1]. This multiplier chain delivers 0 dBm output power with 92.5 mW DC power consumption. The power efficiency of is around 1% [4.3-1], which is defined as $\eta = \frac{P_{out}}{P_{in}+P_{DC}}$, P_{out} is the output power at desired frequency, P_{in} is the input power, and P_{DC} is the DC power consumption of whole multiplier chain. Another W-band frequency sixtupler presented in[4.3-2] consists of a passive frequency tripler/doubler utilizing Schottky diode, as well as a buffer amplifier. This sixtupler consumes 125 mW DC power, obtaining output power of -5 dBm. It has a power efficiency of 0.24%.

In [4.3-1] a W-band frequency multiplier-by-eight (x8) is presented, which consists of 3 frequency doublers and two active baluns, as shown in Figure 33. This multiple chain is able to deliver 6.8 dBm output power with DC power consumption of 600 mW. Its power efficiency is 0.81%. In their design, doublers are made of a transistor pair on push-push configuration, as shown in Figure 34. Alternatively, doublers based on Gilbert cell are used in a frequency multiplier-by-eight [4.3-5]-[4.3-6]], as shown in Figure 35. Comparing with push-push configuration, the Gilbert cell doubler has better conversion gain, thus, no buffer amplifier between doublers is needed. Of course, the Gilbert cell consumes more DC power than a push-push configuration due to double balanced configuration. The frequency multiplier-by-eight in [4.3-5] is able to deliver 3 dBm output power at 140 GHz with a DC power consumption of 178 mW, which has a power efficiency of 1.1%.

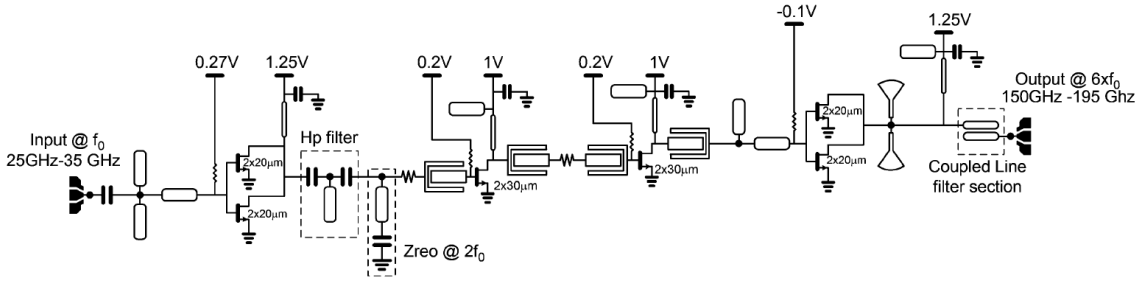

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Figure 32: Schematic diagram of a multiplier-by-six [4.3-1]

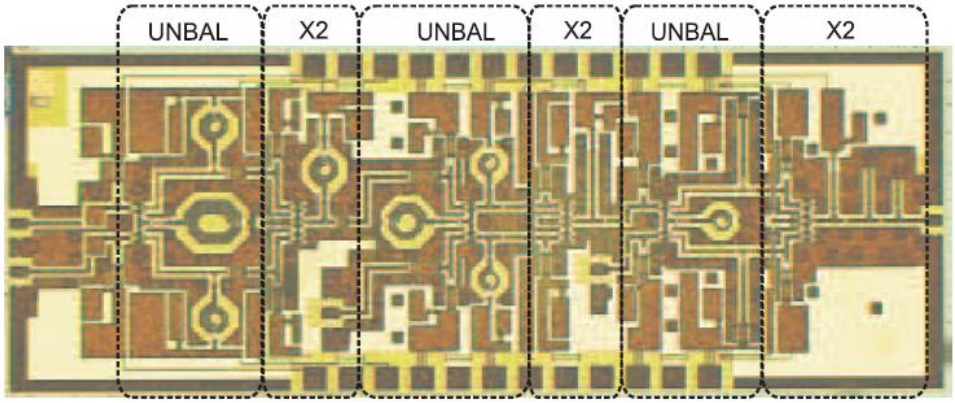

Figure 33: Chip photograph of the W-band frequency multiplier-by-eight MMIC. Chip size is $1.5\times4mm^2$ [4.3-4]

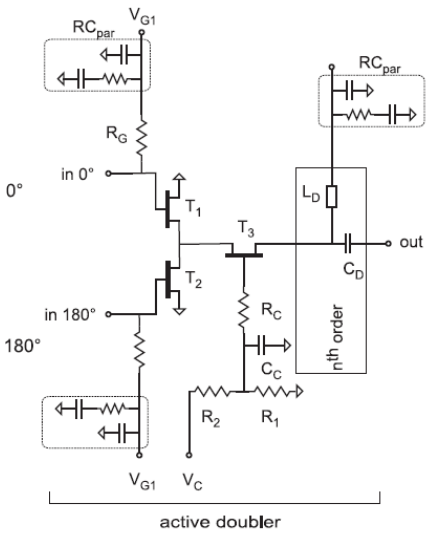

Figure 34: Double with push-push configuration [4.3-4]

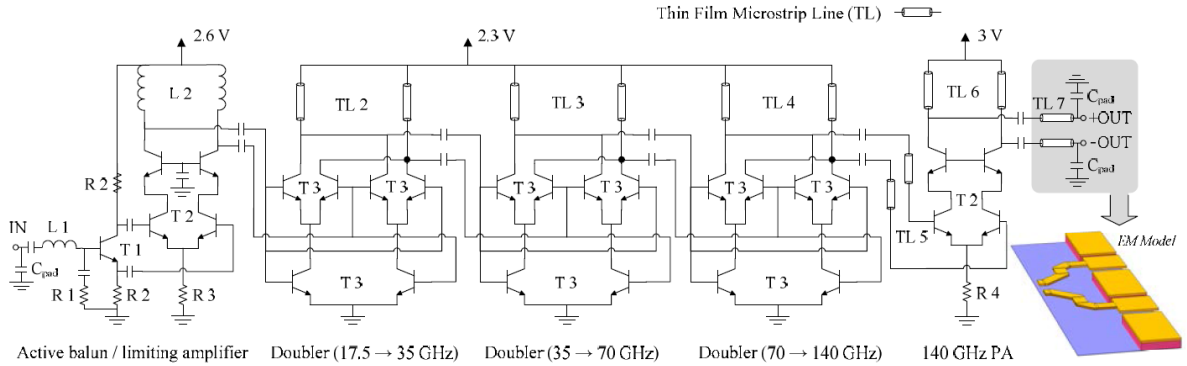

Figure 35: F-band frequency octupler [4.3-5]

It is a challenge to design frequency multipliers with low DC power consumption (< 70mW) and high power efficiency (>4%). The output power is between 2 to 5 dBm. In order to avoid power losses due to balun's amplitude/phase unbalance and to reduce the complicity of the circuit, single-ended topologies are chosen in our design. Moreover, a simple L-type inter-stage matching network is applied, which consists of a inductor at collector (one terminal is ac grounded), as well as a capacitor and a inductor in series. This L-type inter-stage has a function of filter (high-pass), featuring of low losses. Consequently, the designed frequency multipliers have a potential of low DC power consumption and high power efficiency.

4.3.2 D-band frequency multiplier-by-six (x6)

4.3.2.1 Circuit schematics

The frequency multiplier-by-six designed here consists of four cascaded transistors, as shown in Figure 36. Each of transistors is common-emitter configured. The first and the second cascaded transistors form a frequency tripler. The third and the fourth transistors form a frequency doubler. Two neighbouring transistors are connected by a T-type matching network which consists of a capacitor and an inductor in series, as well as an inductor at the collector (for example, C_2 and L_{b2}, L_{c1}).

The frequency tripler using two cascaded common-emitter transistors achieves good power efficiency [4.3-3]. The first transistor is a harmonic generator, which products the fundamental, the second and the third harmonics. While, the second transistor can generate the third harmonic through different mechanisms: 1) mixing the fundamental and the second harmonic; 2) tripling the fundamental 3) amplifying the third harmonic. The third harmonics obtained from different mechanisms add in favourably phase, and consequently improving the tripler's conversion gain. The cascaded frequency doubler generates the desired the sixth harmonic, as the input is dominated by the third harmonic.

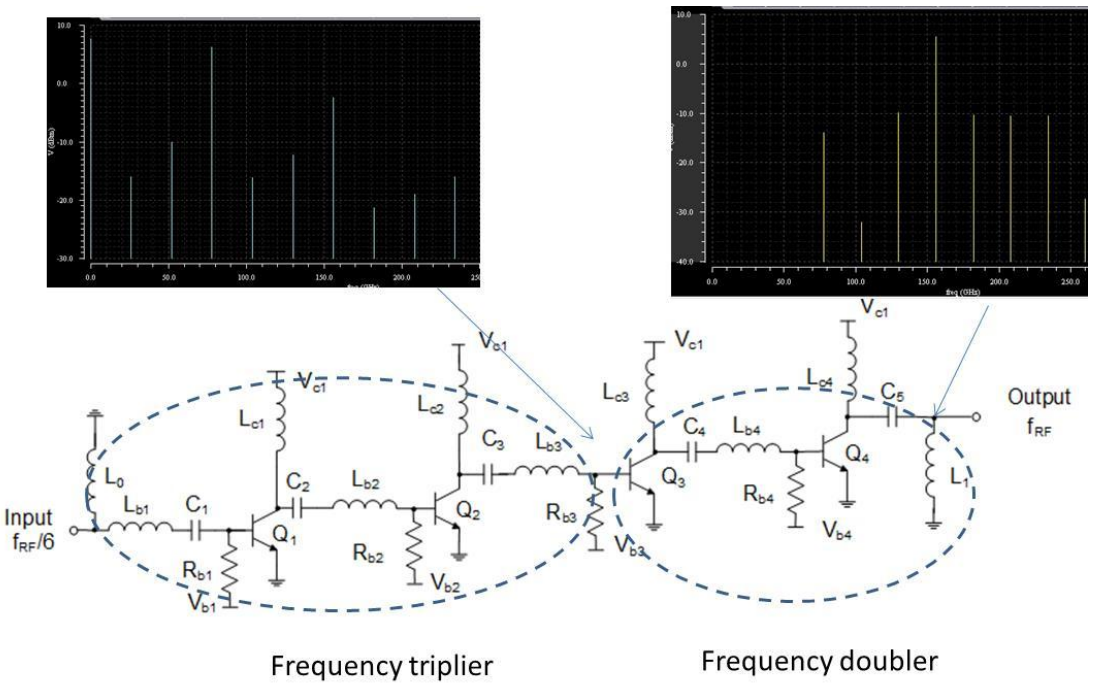

Figure 36: Schematic of the frequency multiplier-by-six

In the design, all base bias voltages, the transistor's sizes, as well as the inductances/ capacitances of the reactive components are determined by optimization in ADS harmonic-balance simulator, in terms of the output power and the suppression of the undesired harmonics, as well as the power efficiency.

The collector supply voltage is 1.0 V. Layout of the multiplier is shown in Figure 37. Chip size is 0.715 mm^2.

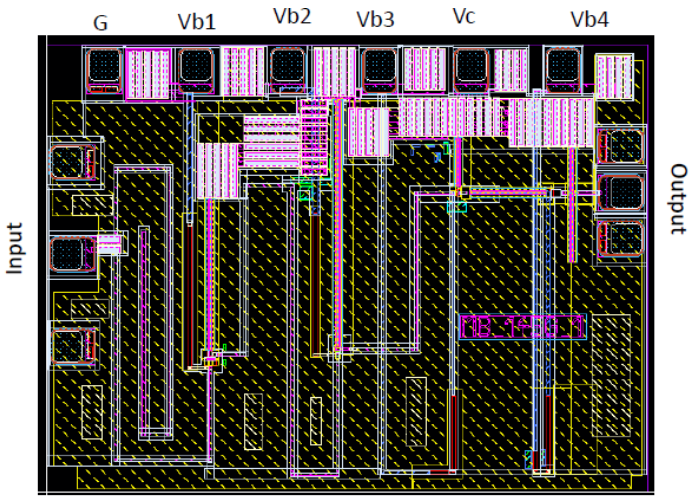

Figure 37: Layout of the frequency multiplier-by-six (size: 0.98x0.73 mm^2)

4.3.2.2 Simulation results

Two simulated output spectra are plotted together in Figure 38. The input signal has a frequency of 24.7 GHz in one simulation; and 27.3 GHz in the other simulation. The frequencies of the output signals are 148.2 and 163.8 GHz correspondingly. Each input has a power of 1.5 dBm. The frequency multiplier-by-six has conversion gain of 3.4 dB with a DC power consumption of 64 mW. Accordingly, the power efficiency is about 5%. Furthermore, the multiplier exhibits more than 10 dB suppression of undesired harmonics. As shown in Figure 39, the 3-dB bandwidth of the multiplier is 20 GHz from 145GHz to 165GHz.

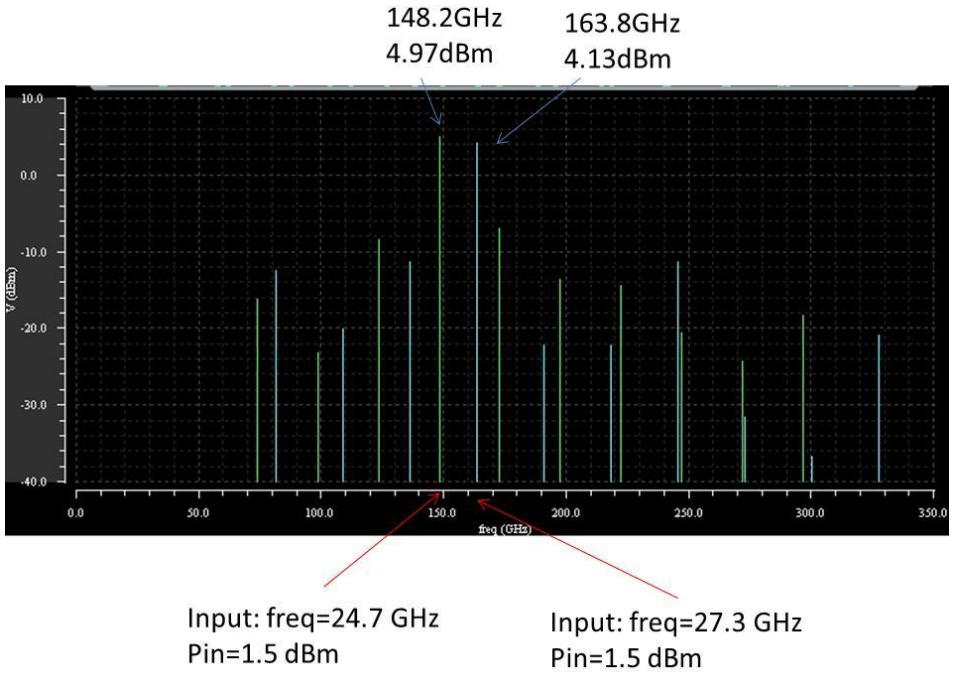

Figure 38: Output spectrum of the frequency multiplier-by-six with two-tone input

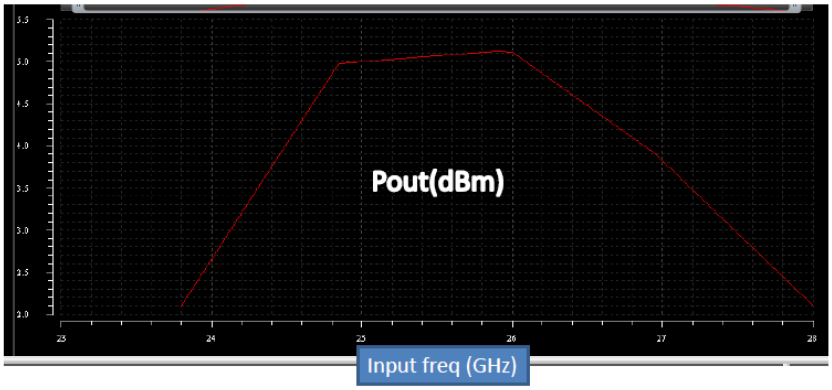

Figure 39: Amplitudes of the sixth harmonic versus the input signal frequency

4.3.3 A G-band frequency multiplier-by-eight (x8)

4.3.3.1 Circuit schematic

The schematic of the frequency multiplier-by-eight designed here is shown in Figure 40, which consists of four common-emitter configured transistors. The first and the second transistor are single-device frequency doubler, which is indicated by the output spectra of the first and the second transistor. The third transistor acts as an amplifier. The last transistor acts as a frequency doubler.

Layout of the frequency multiplier-by-eight is shown in Figure 41. Chip size is 0.72 mm^2.

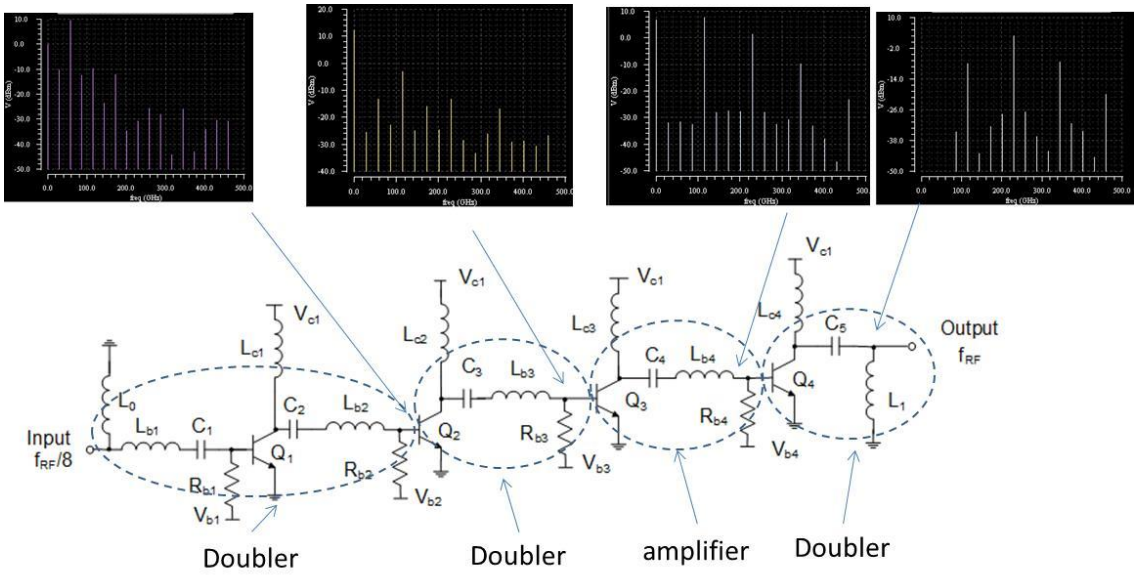

Figure 40: Schematic of the frequency multiplier-by-eight

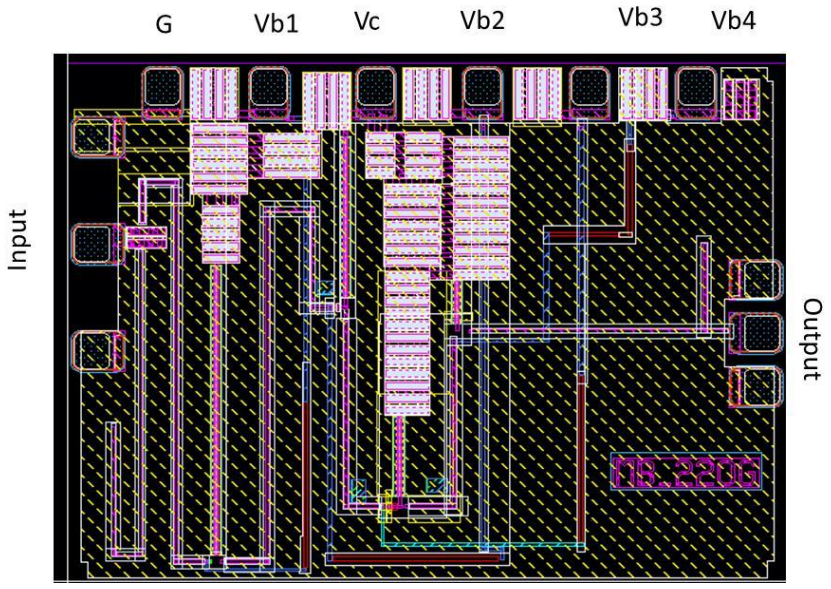

Figure 41: Layout of the frequency multiplier-by-eight, chip size 1.0x0.72 mm^2.

4.3.3.2 Simulation results

Output spectra overlapping 4 simulation-results are shown in Figure 42. Each simulation has an input signal at different frequencies distributed equally between 26.16 and 31.15 GHz. Each input signal has a power of 1.5 dBm. It can be seen that, at output frequencies 209.2 GHz, 219.2GHz, 229.2 GHz, the multiplier has more than 10 dB suppression of the undesired harmonics. The maximum output power is 2.6 dBm at 229.2 GHz. DC power consumption of the multiplier is 39.5 mW with a supply voltage of 1V. The power efficiency is 4.3%. The amplitude of the 8th harmonic versus frequencies of the input signal is plotted in Figure 43. It can be seen that, 3-dB bandwidth is 20 GHz in the frequency range from 208GHz to 228GHz. The maximum conversion gain is 1 dB.

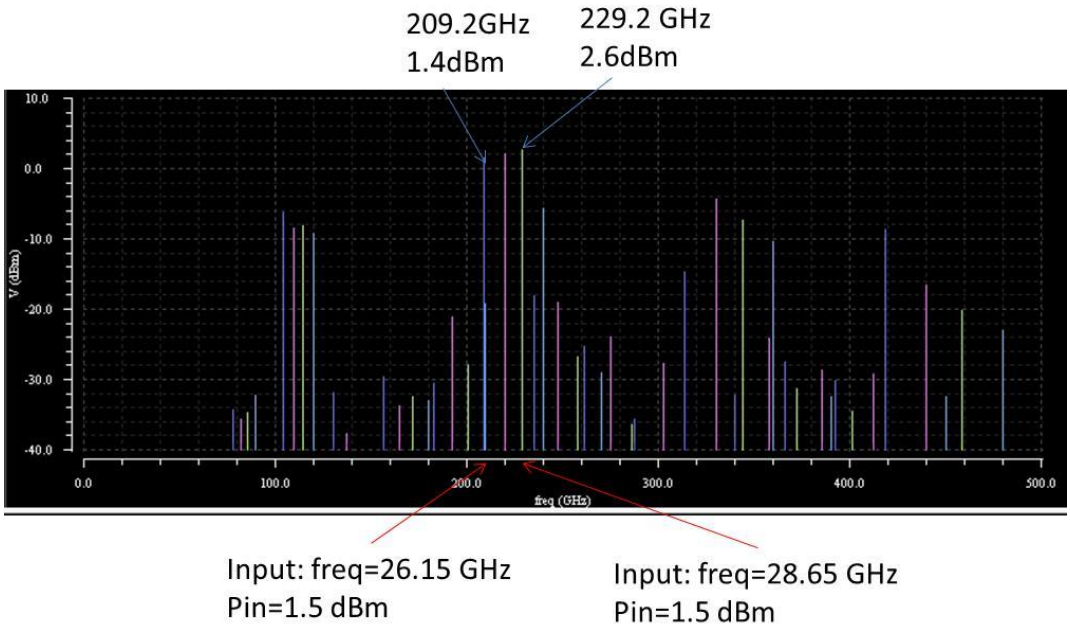

Figure 42: Spectrum of the output signal with 4-tone inputs.

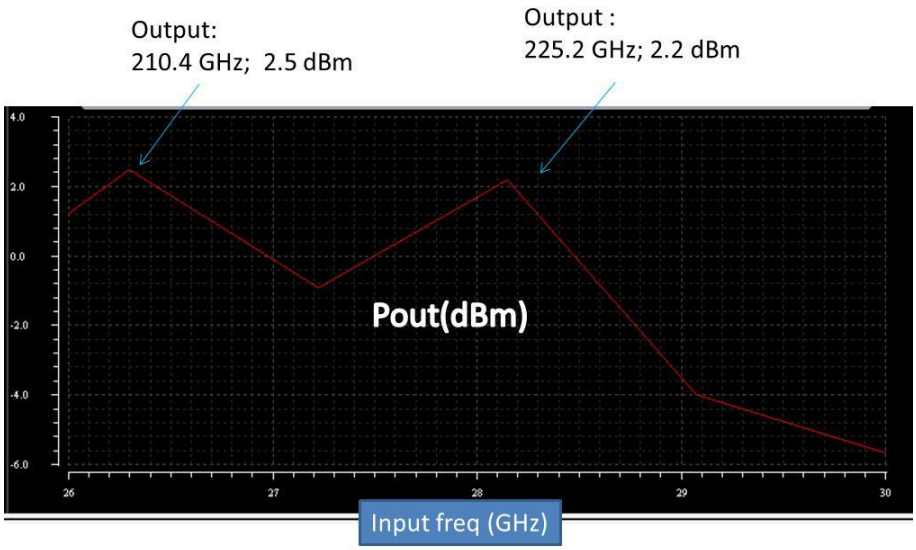

Figure 43: The amplitude of the 8th harmonic versus the frequencies of the input signal

4.3.4 Conclusions

A D-band frequency multiplier-by-six (x6) and a G-band frequency multiplier-by-eight (x8) are designed in a 0.13um SiGe technology. Both multipliers have the same circuit topology, i.e., 4 cascaded common-emitter transistors. Output powers of 5 dBm and 2.5 dBm are obtained at D-band and G-band, respectively, with DC power consumption below 63 mW. Both multipliers have high power efficiency (4~5 %).

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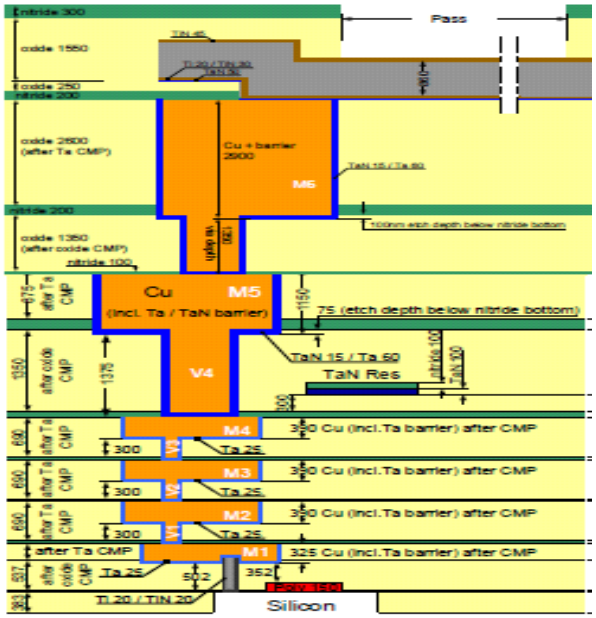
4.4 MMIC to Silicon platform Interface

4.4.1 Technical challenge of MMIC-platform interconnection

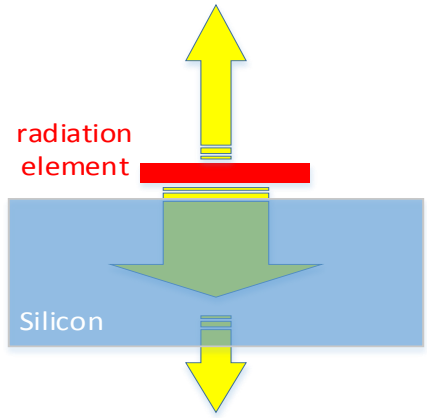
The silicon platform provided by KTH has the advantages of providing different unique passive waveguide components, such as filter, switch, power splitter, etc. The development of an efficient MMIC to silicon platform interconnection solution is one of the critical task in the project.

In this project, we are focusing on non-galvanic interconnection between MMIC and the platform, namely, the signal from the MMIC will be coupled into the waveguide structure simply by EM radiation. Therefore the interconnection design comprises two parts: designing a radiation structure on the MMIC and designing a launching structure to excite waveguide mode effectively.

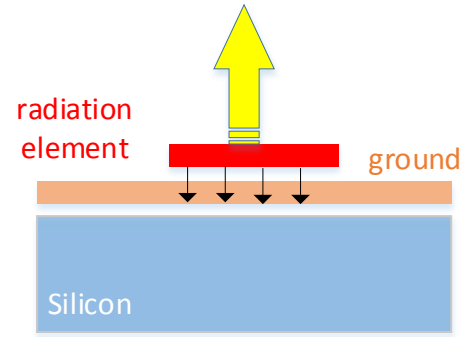
In this project, the MMIC design is made based on the B11HFC SiGe process, there is an intrinsic technical challenge of radiation structure design on this process. The B11HFC SiGe process has six metal layers over a 100um lossy silicon substrate (6-7 Siemens/m), the cross-section diagram of this technology is shown in Figure 4.4.1(a). The radiation element can be implemented on one of the metal layers, however, there are only two possible radiation element configuration can be made over this process as shown in Figure 4.4.1(b-c). On the left hand side, the first configuration is illustrated where the radiation element is implemented on one of the metal layer which is directly facing the air and silicon substrate. In this case, majority radiation energy will be attracted into the silicon substrate due to its dielectric constant is significant higher than air's. Due to the substrate loss, only a fractional radiation energy will pass through substrate. The radiation efficiency of this configuration is limited by the Silicon substrate. On the right hand side, an alternative configuration is presented where a ground layer is used to isolate the radiation element from the substrate. In this case, the substrate will not affect the radiation, however, the distance between metal layers are between 0.5 – 1.3 um, with the ground under than radiation element, the radiation energy to the air will be much less compared to the EM field trapped between the radiation element and the ground. It can be seen in both configurations, building an effective radiation structure on this process is not easy. Previously reported work [4.4.1] using the first configuration, but solved this problem by etching off the silicon under the radiation element. This will require significant post-process efforts or major modification from standard process.



(a)



(b)



(c)

Figure 44: possible radiation element configurations based on B11HFC SiGe process

4.4.2 Proposed of MMIC-platform interconnection concept

Two interconnection concepts have been proposed and studied, one concept is for interconnection between the air-filled waveguide and the MMIC, the other concept is for interconnection between MMIC and high- resistance (low loss) silicon-filled waveguides.

4.4.3 Proposed of MMIC to silicon-filled waveguide interconnect concept

4.4.3.1 The structure of the interconnect concept

As previously mentioned, when the radiation element is directly facing the silicon substrate, most radiation energy will be absorbed in the silicon. This is due to high dielectric constant contrast between silicon and air. To overcome this problem, a concept is proposed where a silicon-filled waveguide is used instead of an air-filled waveguide. When silicon-filled waveguide is closely attached to the MMIC, the radiation element is facing silicon material on both sides (substrate and silicon waveguide), therefore, the energy will equally spread between substrate and waveguide. In order to improve the transition efficiency, directive radiation element should be used, in order to effectively direct energy into waveguide. A U-slot based radiation element is used in the study of this concept [4.4.2].

A drawing of this concept is presented in Figure 45.The MMIC is up-side-down placed on top of a Silicon filled waveguide. On the SiGe MMIC, a microstrip line on metal4 is the radiation element, and a U-slot is implemented on the top metal (metal 6). The U-slot would directed the radiation away from the substrate silicon and insert silicon-filled waveguide. This MMIC is closely attached to the silicon-filled waveguide. The waveguide is made from a high-resistance silicon block with metalized surfaces.

4.4.3.2 Concept Verification

The proposed concept is simulated in HFSS, the result shows the concept can cover entire D-band (110-170 GHz), the insertion loss is 0.4 dB at the center and 0.8 dB at the edge of the band. The simulation result is shown in Figure 46.

4.4.3.3 Challenges during manufacture process

- ***MMIC manufacturing***

  The MMIC design on B11HFC process must yield special design rules to achieve certain metal density requirement for each metal layer. The U-slot size need to be carefully designed, which size should be small enough to reach minimal local metal density requirement, yet without compromise EM performance. The feeding network under the slot should also be carefully designed with the respect of design rule.

- ***Silicon filled waveguide manufacturing***

  The waveguide structure should be filled with high-resistive silicon, whose surfaces have to be metalized. The top surface of the waveguide where is in contacted with the U-slot should not be metalized, this implies a mask should be used for top surface metallization process.

  It is possible to manufacture silicon-filled waveguide as illustrated, however the transition from silicon-filled waveguide to air-filled waveguide will be difficult to implement. Therefore it is hard to make this concept compatible with any tunable / reconfigurable components designed in the air-filled waveguide.

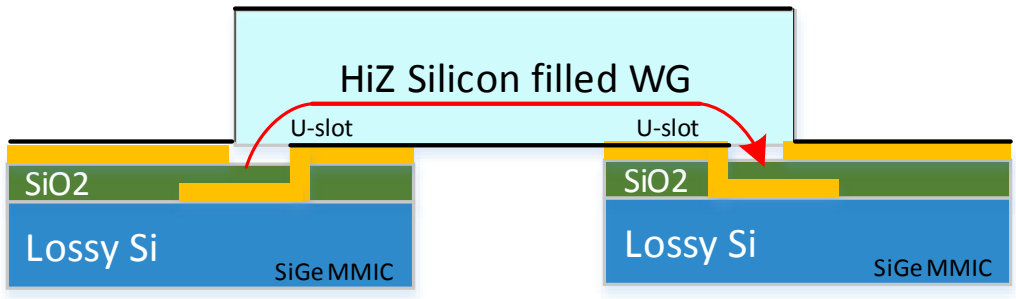


Figure 45: Proposed MMIC to silicon filled waveguide interconnection concept

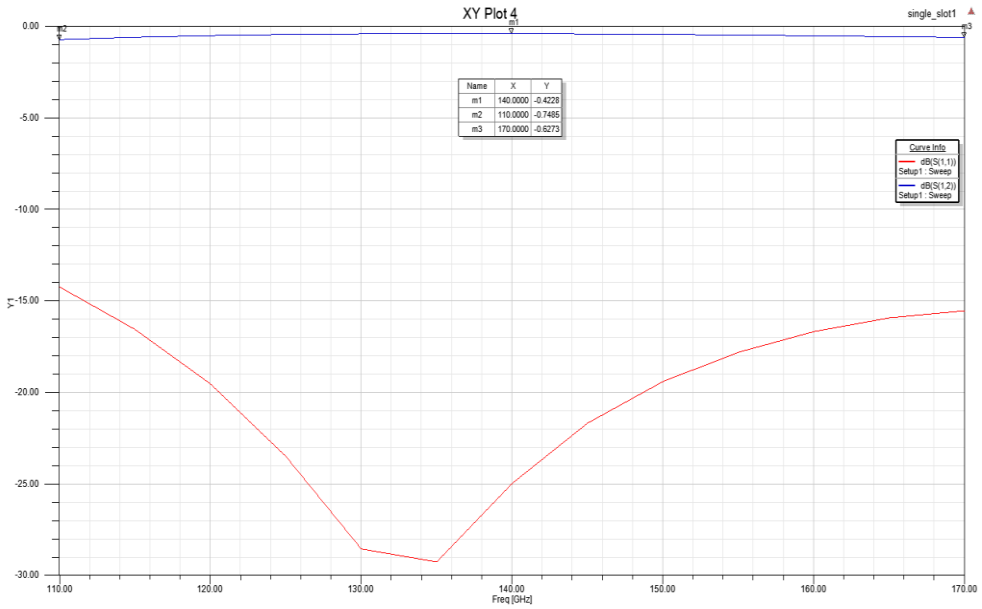


Figure 46: Simulated result of the MMIC to silicon filled waveguide interconnection concept

4.4.4 Proposed of MMIC to air-filled waveguide interconnect concept

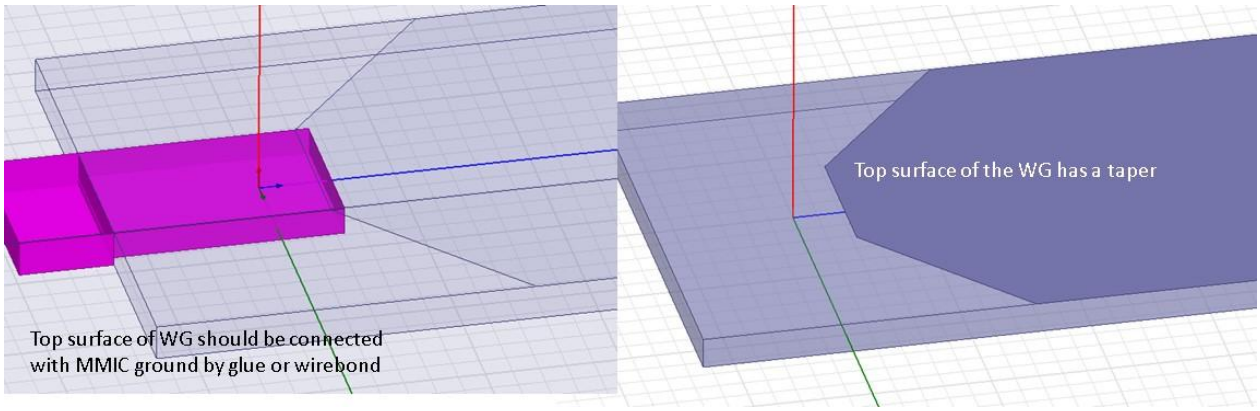
4.4.4.1 The structure of the interconnect concept

The structure concept mentioned above tried to use silicon based waveguide to reduce the proportion of energy that radiates into the substrate. This concept as an alternative, place the MMIC into an air-filled waveguide to utilize the energy radiated to the air and radiated through the substrate. The structure is shown in Figure 47 (a).

On the MMIC, a U-slot is placed at Metal 1 (the metal closest to the substrate), with this slot, it is possible to direct the EM radiation pass through the substrate via shortest path in the lossy substrate. The feeding radiation element is placed at metal 4 which will radiate into the air and the slot simultaneously. To utilize the energy radiated into the air, the top surface of the waveguide should be located as close as to the MMIC (also to the feeding radiation element). In order to exciting waveguide mode from the MMIC, a transition is made on the top surface of the waveguide as shown in Figure 47 (b). The waveguide has an opening on its top surface, and this surface has a taper shape. The end of the taper is either glued or wire-bonded to the ground of the MMIC. The U-slot is placed on metal 1, in order to direct the

radiation direction the slot is modified to a butterfly shape as shown in Figure 47 (c). This butterfly shape also ensure a good matching over wide frequency band.

(a)



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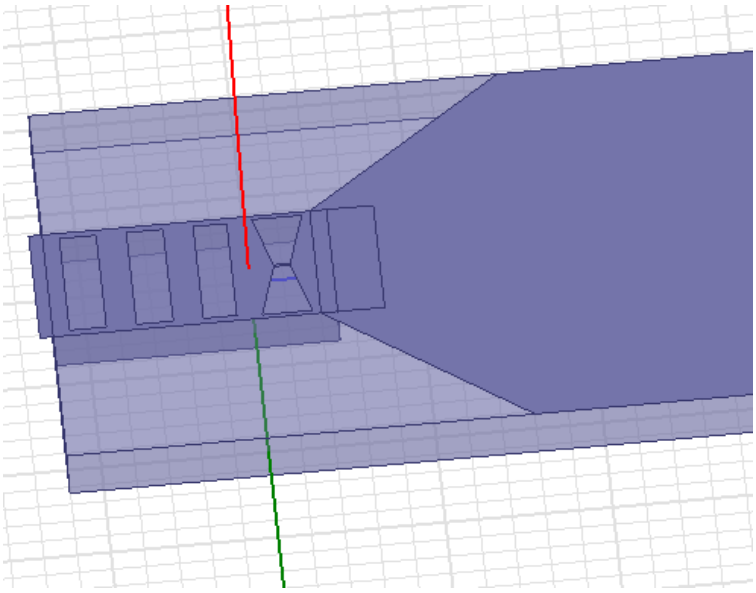

(c)

Figure 47: Illustration of the MMIC to air filled waveguide interconnection concept: (a) side-view of the structure. (b) Top surface of the waveguide and its positioning to the MMIC. (c) a butterfly shape slot design on the MMIC metal1.

4.4.4.2 Concept Verification

The proposed concept is simulated in HFSS, the result shows the concept can cover entire D-band (110-170 GHz), the insertion loss is 1.4 dB at the center and 2.5 dB at the edge of the band. The simulation result is shown in Figure 48. Due to the loss in the substrate, this

concept yield higher insertion loss compared to the first concept, however, air-filled waveguide is easier to manufacture compared to the silicon-filled one.

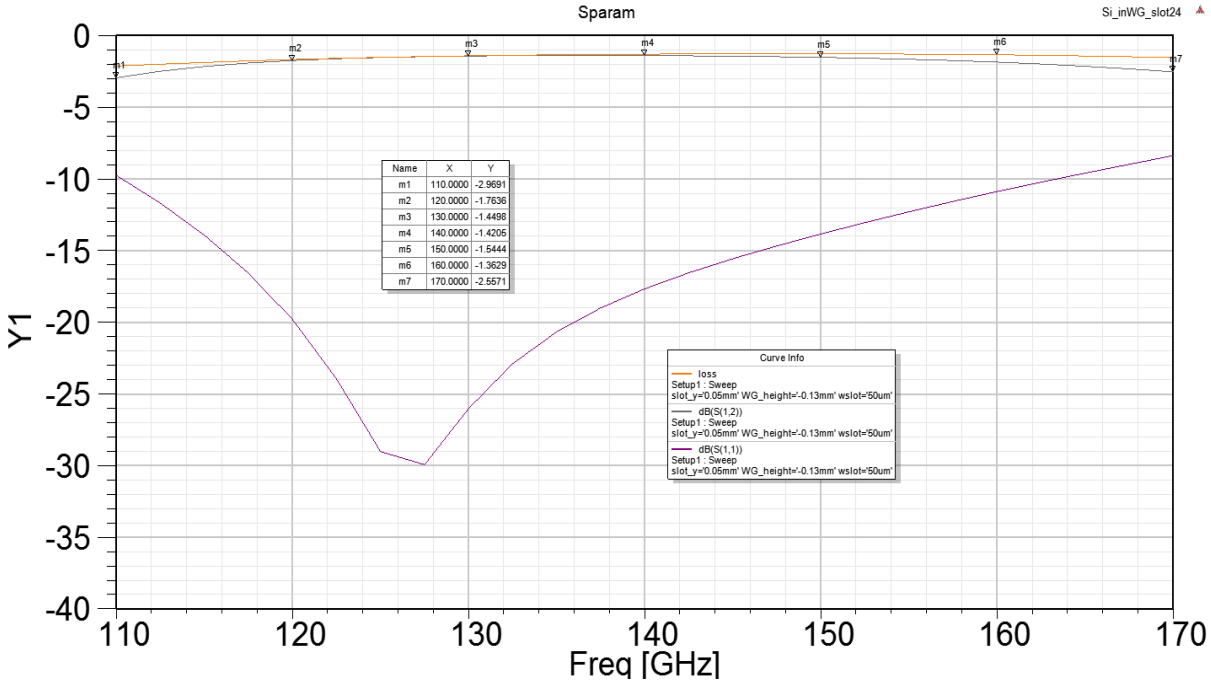

Figure 48: Simulated result of the MMIC to air filled waveguide interconnection concept

4.4.4.3 Challenges during manufacture process

- ***MMIC manufacturing***

  The MMIC design is challenging for this concept, because the radiation element shall radiate into the air and through the substrate simultaneously. As shown in figure. 4.4.4 (c), the butterfly shape slot on metal 1 should be carefully tailored to avoid violate design rule.

- ***Waveguide manufacturing***

  The air filled waveguide is possible to be manufactured on the silicon platform, however, the height of the waveguide is lower compared to the standard waveguide. This may cause compromise on the performance. The taper structure is possible to achieve, and it is possible to glue the MMIC to the taper. Though the position accuracy of assembling needs to be investigated.

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Chapter 5 Summary and conclusion

The deliverable D3.3 defines the module architecture of the wireless millimeterwave communication demonstrator as well as a steerable antenna based on MEMS-phase-shifter. An architecture for the transmitter and receiver MMIC chipset (TX/RX) based on specification from telecom industry is defined and concepts/solutions for the realization of the sub-circuits are proposed in detail, including simulations and layout for some circuits (LNA and frequency multiplier). Simulation results show following key data:

A proposed 6-stage, common source, LNA shows a simulated gain of. 18.9 dB, and very large 1dB bandwidth of 117-162 GHz with an associated noise figure of 10.2 dB. A cascade based 3 stage LNA (2 cascode stages followed by a CE-stage), shows a gain of 18.5 dB, with a noise figure of 9.8 dB, with a 3dB bandwidth is 126-160 GHz.

A D-band frequency multiplier-by-six has a conversion gain of 3.4 dB with a DC power consumption of 64 mW and a power efficiency is about 5%. The multiplier exhibits more than 10 dB suppression of undesired harmonics. The 3-dB bandwidth of the multiplier is 20 GHz from 145GHz to 165GHz.

Two interconnection concepts have been proposed and studied, one concept is for interconnection between the air-filled waveguide and the MMIC, the other concept is for interconnection between MMIC and high- resistance (low loss) silicon-filled waveguides.

An insertion loss of 1.4dB is obtained for the interconnection to the air-filled waveguide at the center of the D-band, at 140 GHz. The interconnection to the silicon filled waveguide has an insertion loss of 0.4 dB at the center of the D-band.

References to published results and a review to the state-of-the-art is given for the sub-circuits of the TX/RX chipset, namely low noise amplifiers, power amplifiers, mixers/modulators, and LO-frequency multipliers.

So far, the initial simulation results are well aligned with the specifications and state-of-the-art, compared to the same technology node.

Chapter 6 List of Abbreviations

COTS	Commercial-off-the-shelf
DC	Direct Current
FCC	Federal Communications Commission
FDD	Frequency Division Duplex
Gbps	Gigabit per second
IF	Intermediate Frequency
InP	Indium Phosphide
I-Q	In-phase - Quadrature-phase
LNA	Low Noise Amplifier
LO	Local Oscillator
MEMS	Micro-Electro-Mechanical System
MMIC	Monolithic Microwave Integrated Circuit
PA	Power Amplifier
PLL	Phased Locked Loop
Psat	Saturated output power
PtP	Point to Point
RF	Radio Frequency
RX	Receiver
SiO2	Silicon Dioxide
SiGe	Silicon Germanium
SSB	Single Sideband
TBD	To Be Determined
TDD	Time Division Duplex
TX	Transmitter
WG	Waveguide